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CHANNEL SELECTION IN DIGITAL TELEVISION

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- (*) Notice: This patent issued on a continued prosecution application filed under 37 CFR

1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C.

154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/406,541

Filed: Sep. 27, 1999 (22)

(65)**Prior Publication Data**

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- Int. Cl.⁷ H04N 5/445; H04N 5/54; H04N 7/00; H04N 5/50
- 348/563; 725/57; 725/56
- Field of Search 348/731, 734, 348/385.1, 386.1, 569, 906, 563, 553, 732, 570; 725/56, 44, 151, 20, 57

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ABSTRACT

Methods and apparatus implementing a technique for selecting a channel in a digital television. In one implementation, selecting a channel includes: receiving a major and minor channel number sequence, including a major channel number, a delimiter, and a minor channel number, where the delimiter separates the major channel number and the minor channel number; identifying a physical channel which corresponds to the major and minor channel number sequence by accessing a channel look up table, where the channel look up table includes correspondences between major and minor channel number sequences and physical channels; identifying a virtual channel table which corresponds to the physical channel, where the virtual channel table indicates a virtual channel which corresponds to the major and minor channel number sequence; tuning to the physical channel to receive a signal carried on the physical channel; and decoding the virtual channel from the tuned signal.

18 Claims, 7 Drawing Sheets

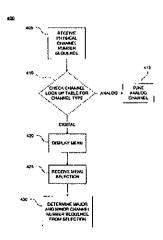


FIG. 1A

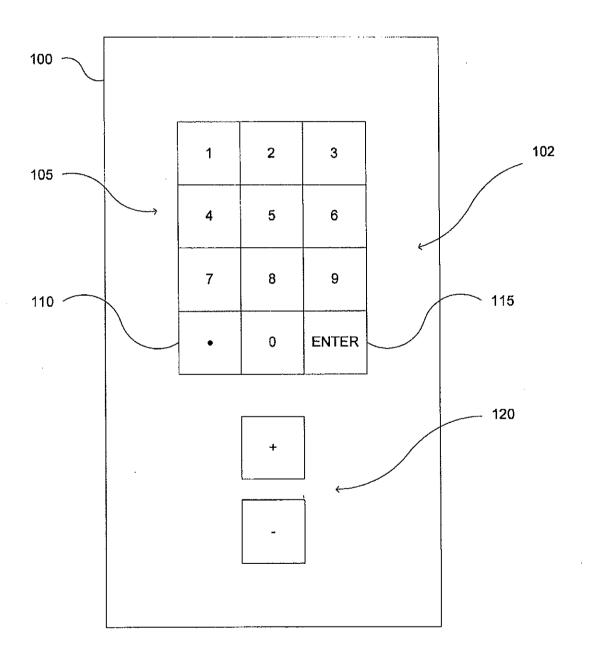


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FIG. 1B

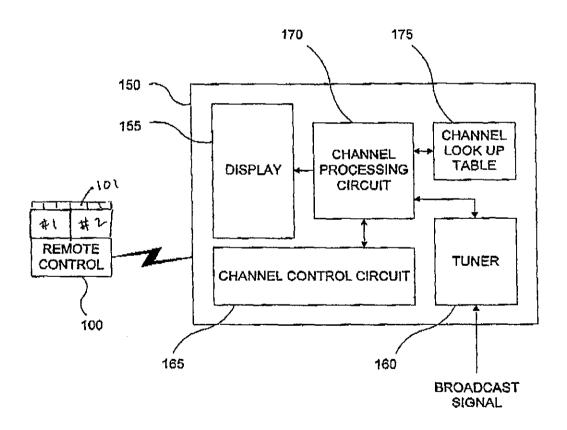


FIG. 2A

<u>200</u>

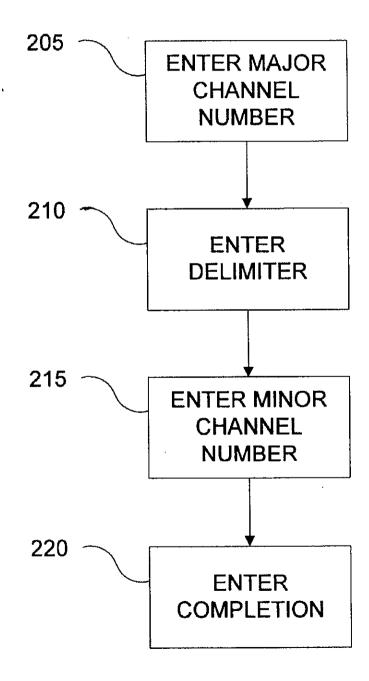
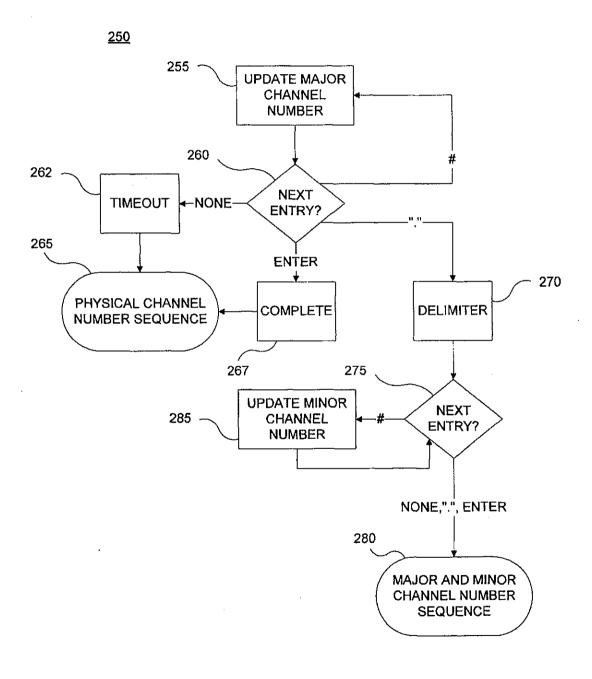


FIG. 2B



U.S. Patent

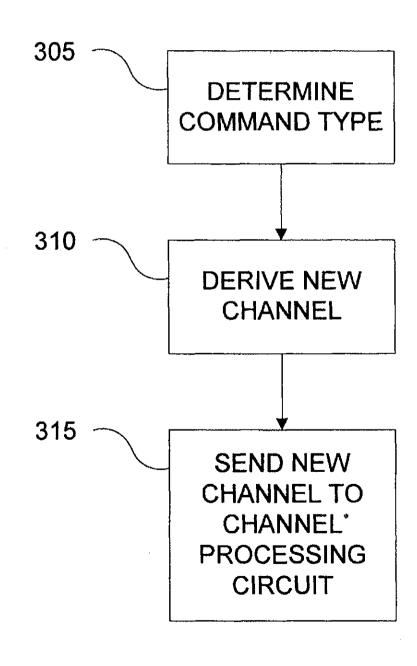
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FIG. 3

<u>300</u>



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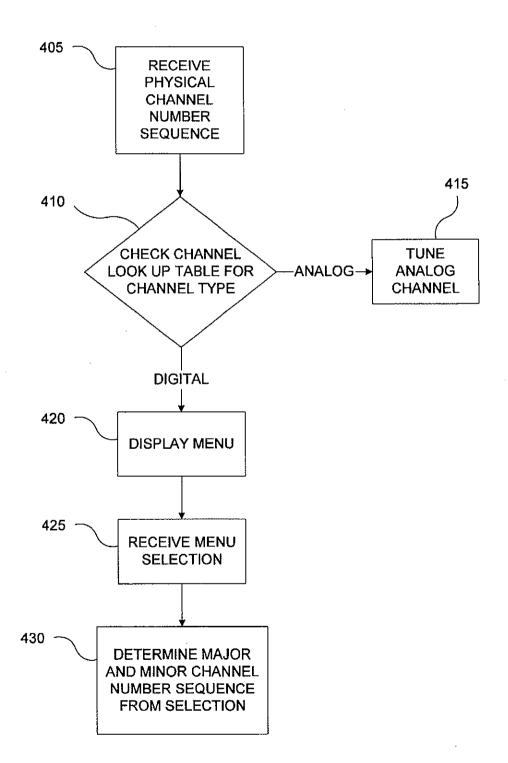
Dec. 9, 2003

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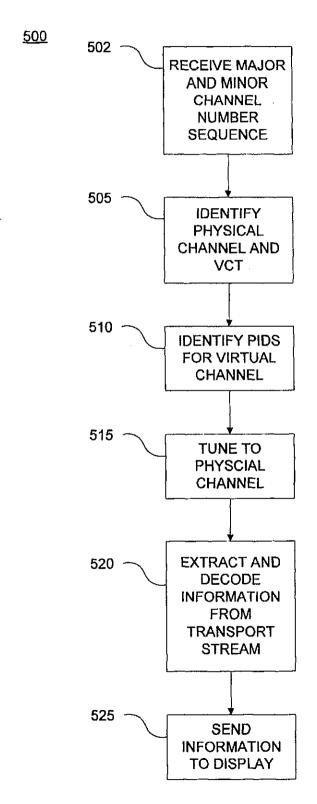
FIG. 4

<u>400</u>



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FIG. 5



CHANNEL SELECTION IN DIGITAL **TELEVISION**

This application claims the benefit of U.S. Provisional Application No. 60/102,942, filed Sep. 30, 1998.

BACKGROUND

To view a television program being transmitted to a user's television, the user provides a channel number to the television. In conventional analog broadcast television, this 10 channel number is a reference to a particular frequency band at which the analog signal carrying the television program is broadcast. This frequency band is also referred to as a "physical channel." The channel number identifies from which frequency band a tuner in the television is to receive. 15 display. Thus, a channel number indicates a physical channel and the associated program.

In digital broadcast television, a frequency band can carry a signal which is an encoded digital transport stream. When decoded, the transport stream can include one or more 20 streams having various forms of content, such as video or audio for a program, text based information, closed captioning, or any information which can be transmitted digitally. Each of these items can be associated with a different channel number. Accordingly, a single physical 25 channel can include multiple items or "virtual channels." In this case, a channel number refers to a virtual channel, a particular item encoded within a transport stream, instead of referring to a physical channel.

In addition, content in a transport stream can be related to 30 content broadcast as an analog signal or in a different transport stream. For example, a transport stream can include a high definition television ("HDTV") version of a program that is also broadcast as an analog signal at a different unrelated frequency band.

SUMMARY

The invention provides methods and apparatus implementing a technique for selecting a channel in a digital television. In one implementation, selecting a channel 40 includes: receiving a major and minor channel number sequence, including a major channel number, a delimiter, and a minor channel number, where the delimiter separates the major channel number and the minor channel number; identifying a physical channel which corresponds to the 45 channel. major and minor channel number sequence by accessing a channel look up table, where the channel look up table includes correspondences between major and minor channel number sequences and physical channels; and identifying a virtual channel table which corresponds to the physical 50 channel, where the virtual channel table indicates a virtual channel which corresponds to the major and minor channel number sequence. Selecting a channel can further include: tuning to the physical channel to receive a signal carried on the tuned signal.

In another aspect, an input device for selecting a channel in a digital television includes: a keypad including a plurality of number keys for inputting respective numbers; and a delimiter key for inputting a delimiter, where a channel is 60 indicated by a major and minor channel number sequence which includes a major channel number input through one or more number keys of the keypad, a delimiter input through the delimiter key, and a minor channel number input through one or more number keys of the keypad.

In another aspect, a digital television includes: a display; a tuner including a connection for an externally supplied

broadcast signal, where the tuner provides a signal carried on a physical channel selected from the broadcast signal; a channel control circuit which derives major and minor channel number sequences from received control signals, where a major and minor channel number sequence indicates a specific channel carried in the broadcast signal; a channel processing circuit connected to the channel control circuit, the display, and the tuner, where the channel processing circuit causes the tuner to select a physical channel corresponding to the major and minor channel number sequence supplied by the channel control circuit and provide a digital signal carried thereon, decodes a channel indicated by the major and minor channel number sequence in the digital signal, and supplies the decoded channel to the

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A shows a hand-held remote control which provides efficient input of major and minor channel numbers to select a channel on a digital television.

FIG. 1B shows a remote control and a digital television. FIG. 2A is a flowchart of a process for directly entering channel numbers for a major and minor channel number sequence using a keypad.

FIG. 2B is a flowchart of a process for processing number sequences entered using a keypad.

FIG. 3 shows a process for selecting a channel using channel commands.

FIG. 4 is a flowchart of a process for selecting a virtual channel through a menu shown on a display.

FIG. 5 is a flowchart of a process for processing major and minor channel number sequences in a digital television.

DETAILED DESCRIPTION

The Advanced Television System Committee ("ATSC") established a standard protocol for transmission of data tables for use with digital television. This protocol is referred to as the Program and System Information Protocol ("PSIP") and is described in "Program and System Information Protocol for Terrestrial Broadcast and Cable," document A/65, Dec. 23, 1997 published by the ATSC. The information describing the content of a transport stream for a physical channel is referred to as the PSIP for that physical

In digital television, each channel in a transport stream is a virtual channel associated with a major channel number and a minor channel number. A major channel number can be used to identify channels which belong to a common broadcast corporation or other group. A minor channel number specifies a particular channel in such a group. In one example, all the virtual channels in a transport stream have the same major channel number and have respective minor channel numbers. In addition, virtual channels can have as the physical channel; and decoding the virtual channel from 55 a major channel number the channel number of a physical channel carrying a related analog channel (analog channels do not need minor channel numbers). In another example, a program is transmitted as an analog signal on physical channel 2. The HDTV version of the same program is transmitted in a transport stream, such as within an unrelated frequency band on a different physical channel, and the virtual channel for that HDTV program has the major channel number 2. Thus, a physical channel can be indicated by a major channel number and a virtual channel can be indicated by a major and minor channel number pair.

The PSIP describes the information for all the virtual channels in a transport stream. The PSIP includes a virtual

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channel table ("VCI") which describes the correspondence between major and minor channel numbers and the virtual channels. A digital television uses the VCT to interpret a user's input to select the appropriate major and minor channel number and hence the desired virtual channel.

FIG. 1A shows an implementation of an input device as a hand-held remote control 100 which provides efficient input of major and minor channel numbers to select a channel on a digital television. Remote control 100 includes at least one keypad 102. Keypad 102 includes one or more number keys 105, such as 10 number keys labeled 0-9, a delimiter key 110, an enter key 115, and one or more channel command keys 120, such as keys labeled with plus ("+") and minus ("-"). In an alternative implementation, a keypad includes alphanumeric keys so that a user can enter combinations of letters and/or numbers to identify a channel, such as "SNN.HDTV". Alphanumeric labels can be set by the user or provided automatically, such as through a broadcast signal in a transport stream.

A user enters channel numbers by depressing one or more number keys 105. A user indicates the separation between a major channel number and a minor channel number by depressing delimiter key 110. A sequence of a major channel number, a delimiter, and a minor channel number is a major and minor channel number sequence. Because delimiter key 110 is provided on remote control 100, a user can conveniently enter a major and minor channel number sequence to access a specific channel directly.

Delimiter key 110 is marked with a delimiter. In FIG. 1A, delimiter key 110 is marked with a dot ("."). This delimiter can take any form, for example, and not by way of limitation, a slash ("!"), a space (" "), or a dash ("-"). The choice of a dot as the delimiter is advantageous as being a familiar break in numeric representation in the decimal system. In one implementation, the delimiter is implemented as a predetermined break or arrangement of memory storage, rather than a separately stored character. In another implementation, the delimiter is indicated by inputting a major channel number with a first keypad and a minor channel number with a second keypad (shown in FIG. 1B).

To complete a channel number entry, the user can depress enter key 115. An automatic timeout can also complete a channel number entry if the user does not depress any key for a specified period. The user enters channel commands by depressing one of one or more channel command keys 120, such as to change to a sequentially adjacent channel. For example, in one implementation, to change from the current channel to the sequentially next channel, the user can depress a channel command key 120 marked with a plus 50 ("+").

FIG. 1B shows remote control 100 and a digital television 150, with the control 100 potentially having one or more keypads (two shown) and alphabet keys 101. Digital television 150 includes a display 155, such as a cathode ray tube 55 ("CRT"), a tuner 160, a channel control circuit 165, and a channel processing circuit 170. These components can be implemented separately or in combination. In one implementation, digital television 100 also includes an integrated keypad for entry of channel numbers and commands 60 directly into digital television 150.

Remote control 100 sends control signals to digital television 150 according to keys depressed by the user. Channel control circuit 165 receives the control signals. Channel control circuit 165 recognizes channel commands or combinations of channel numbers and delimiters to select a desired physical or virtual channel. For example, in an

implementation where the delimiter is a dot, channel control circuit 165 recognizes the sequence "4.2" as a request for major channel number 4 and minor channel number 2. Channel selection is described further below with respect to FIGS. 2A through 5. Channel control circuit 165 provides channel information, such as major and minor channel numbers, to channel processing circuit 170.

Channel processing circuit 170 uses the channel information from channel control circuit 165 and information stored in a channel look up table 175 to determine the desired physical or virtual channel. Channel look up table 175 is implemented as writeable memory, such as RAM or flash ROM. Channel processing circuit 170 creates channel look up table 175 during initialization of digital television 150 and updates channel look up table 175 dynamically. Channel look up table 175 defines correspondences between major and minor channel numbers and physical and virtual channels. The allocation of minor channel numbers is derived from information obtained from the PSIP of digital physical channels. Major channel numbers correspond to physical channels, which may be different from the physical channels carrying the transport streams. Channel look up table 175 also indicates whether each physical channel is an analog channel or a digital channel.

Channel processing circuit 170 causes tuner 160 to select a physical channel from a broadcast signal received at digital television 150. The broadcast signal can be received through various reception systems, such as an antenna, a cable system (e.g., CATV), or a satellite system (e.g., DSS). Tuner 160 provides a signal on the selected physical channel to channel processing circuit 170.

When the channel information indicates a physical channel is desired, such as an analog channel, channel processing circuit 170 passes the signal from tuner 160 to display 155 unchanged. When the channel information indicates a virtual channel is desired, channel processing circuit 170 performs appropriate digital signal processing to extract information from a transport stream based on information supplied in the VCT. For example, channel processing circuit 170 can extract and decode, using decoding such as MPEG-2, a video signal and an audio signal from a transport stream which corresponds to a desired virtual channel. Channel processing circuit 170 provides the signal or signals to display 155.

FIG. 2A is a flowchart of a process 200 for directly entering channel numbers for a major and minor channel number sequence using a keypad, such as keypad 102 shown in FIG. 1A. A user enters a major channel number by depressing an appropriate number key or keys 105 (205). The user enters a delimiter by depressing delimiter key 110 (210). As discussed above, the delimiter indicates the end of the major channel number. For example, the delimiter allows a user to enter directly and distinguishably the sequences "42.3" and "4.23." The user enters a minor channel number by depressing an appropriate number key or keys 105 on remote control 100 (215). The user completes the sequence by depressing enter key 115 (220). The major channel number, delimiter, and minor channel number can be supplied to the channel control circuit separately or together.

FIG. 2B is a flowchart of a process 250 for processing number sequences entered using a keypad, such as keypad 102 shown in FIG. 1A, to generate a channel number sequence in a digital television, such as in channel control circuit 165 shown in FIG. 1B. As described above, a major and minor channel number sequence includes a major channel number, a delimiter, and a minor channel number. A physical channel number sequence includes a channel number.

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When channel control circuit 165 receives an entry of a channel number, and is not already processing another channel number sequence, channel control circuit stores the received number as the first digit of a current channel number (255). Channel control circuit 165 causes display 5 155 to display the received channel number and entries as entries are received for user feedback. Channel control circuit 165 waits to receive another entry for a specified timeout period (260). If channel control circuit 165 does not receive another entry before the timeout period expires 10 (262), channel control circuit 165 passes the current channel number to channel processing circuit 170 as a physical channel number sequence (265). If channel control circuit 165 receives a completion signal, such as from enter key 115, before the timeout period expires (267), channel control 15 circuit 165 passes the current channel number to channel processing circuit 170 as a physical channel number sequence (265).

If channel control circuit 165 receives another channel number before the timeout period expires, channel control ²⁰ circuit 165 concatenates the new channel number with the current channel number as the next digit (255). Channel control circuit 165 resets the timeout period to wait for another entry (260).

If channel control circuit 165 receives a delimiter before ²⁵ the timeout period expires, channel control circuit 165 concatenates the delimiter with the current channel number (270). Channel control circuit 165 resets the timeout period to wait for another entry (275).

If channel control circuit 165 does not receive another entry before the timeout period expires, channel control circuit 165 passes the current channel number to channel processing circuit 170 as a major and minor channel number sequence (280). If the current channel number ends with a delimiter, channel control circuit 165 concatenates a default value, such as zero, with the current channel number before passing the current channel number to channel processing circuit 170

Similarly, if channel control circuit 165 receives a completion signal, such as from enter key 115, or a second delimiter before the timeout period expires, channel control circuit 165 passes the current channel number to channel processing circuit 170 as a major and minor channel number sequence (280). If the current channel number ends with a delimiter, channel control circuit 165 concatenates a default value, such as zero, with the current channel number before passing the current channel number to channel processing circuit 170.

If channel control circuit 165 receives another channel number before the timeout period expires, channel control circuit 165 concatenates the new channel number with the current channel number as the next digit (285). Channel control circuit 165 resets the timeout period to wait for another entry (275).

For example, to select physical channel 2, an analog channel, a user enters "2" with a number key 105 and then "ENTER" with enter key 115 using remote control 100 as shown in FIG. 1A. To select virtual channel 4.2—the virtual channel which has major number channel 4 and minor channel number sequence (430). FIG. 5 is a flowchart of and minor channel number key 105.

FIG. 3 shows a process 300 for selecting a channel using channel commands, such as using channel command keys 120 as shown in FIG. 1A. When channel control circuit 165 receives a channel command, channel control circuit 165

determines the type of command (305). Channel control circuit 165 recognizes a predetermined set of commands, such as those which are available through remote control 100. Channel control circuit 165 processes the channel command to derive the desired channel (310). Channel control circuit passes the resulting channel number to channel processing circuit 170 as a channel number sequence (315).

An analog channel is sequentially before virtual channels with the same major channel number as the channel number of the analog channel. For example, when channel control circuit 165 has received a "+" command and the currently displayed channel is 4, channel control circuit 165 sends a request to channel processing circuit 170 for the next sequential channel. Channel processing circuit 170 checks whether virtual channel 4.1 is available and, if not, whether analog channel 5 is available, and so on. Channel processing circuit 170 returns the resulting channel number to channel control circuit 165, or alternatively can process the channel number directly.

FIG. 4 is a flowchart of a process 400 for selecting a virtual channel through a menu shown on a display, such as display 155 shown in FIG. 1B. When channel processing circuit 170 receives a physical channel number sequence from channel control circuit 165 (405), channel processing circuit 170 checks in the channel look up table 175 whether the selected physical channel is a digital or analog channel (410). If the physical channel is an analog channel, channel processing circuit 170 causes the tuner 160 to tune to the physical channel to display the broadcast signal on display 150 (415).

If the physical channel is a digital channel, channel processing circuit 170 causes display 150 to display a menu listing one or more virtual channels associated with that physical channel (420). To generate the menu, channel processing circuit 170 accesses the VCT of the transport stream on the physical channel. Alternatively, channel processing circuit 170 generates a full channel list of all the channels, virtual and analog, that have the same major channel number as the major channel number which corresponds to the selected physical channel.

In one implementation, channel processing circuit 170 always generates a full channel list for the selected physical channel, whether the physical channel is analog or digital. For example, in the case of an analog physical channel, channel processing circuit 170 obtains the major channel number corresponding to the selected analog physical channel from the channel look up table 175. Channel processing circuit 170 forms the full channel list by searching channel look up table 175 for all the virtual channels which have that major channel number.

Channel processing circuit 170 receives a selection from the menu made by the user (425). The user can select entries from menus in various ways, such as by using channel command keys 120 shown in FIG. 1A. Channel processing circuit 170 uses channel look up table 175 to find major and minor channel numbers corresponding to the selected entry and uses these numbers as a major and minor channel number sequence (430).

FIG. 5 is a flowchart of a process 500 for processing major and minor channel number sequences in a digital television, such as digital television 150 shown in FIG. 1B. After receiving a major and minor channel number sequence (502), channel processing circuit 170 identifies a physical channel and VCT associated with that sequence using channel lookup table 175 (505). For example, upon receiving the

major and minor channel number sequence "4.2" (i.e., a sequence having major and minor channel numbers 4 and 2, respectively), channel processing circuit 170 accesses channel lookup table 175 to determine the associated physical channel, such as physical channel 39. Channel processing 5 circuit 170 also accesses the VCT for physical channel 39 such as through a pointer to the VCT stored in channel lookup table 175. Channel processing circuit 170 retrieves one or more packet identifiers ("PIDs") from the accessed VCT for packets in the transport stream on the selected physical channel which correspond to the selected virtual channel (510). As described above, a major and minor channel number sequence indicates a virtual channel. A single virtual channel can have associated multiple information streams. For example, the VCT may indicate that video data for the selected virtual channel has one PID and 15 audio data has another PID.

Channel processing circuit 170 causes tuner 160 to tune to the selected physical channel (515). Channel processing circuit 170 extracts and decodes appropriate information from the signal received on the tuned physical channel using 20 the retrieved PID or PIDs (520). Channel processing circuit 170 supplies this information to display 155 (525). Channel processing circuit 170 can also supply audio or other information to appropriate components of digital television 150.

The invention can be implemented in, or in combinations 25 of, digital electronic circuitry, computer hardware, firmware, or software. An implementation can include one or more stored computer programs executable by a programmable system including a programmable processor and memory.

In the implementations described above, information 30 describing virtual channels and mapping between channel numbers and virtual channels and physical channels is carried in the PSIP of digital channels. In alternative implementations, however, this information can be supplied in various ways or in a combination of ways. This mapping information can be provided by out-of-band ("OOB") 35 signaling, such as in CATV. Alternatively, the mapping information can be provided by in-band signals, such as program guide and mapping information provided on a portion of an analog or digital channel. The information can be provided in real time or periodically, on a single channel or multiple channels. For example, in one such implementation, the channel processing circuit of a digital television builds the channel look up table by combining the mapping information received on multiple channels. A person of ordinary skill in the art will know how to modify the 45 components of the digital television described above to accommodate one or more of these alternative information sources, such as by including additional tuners or software to access and store the mapping information.

In another alternative implementation, the channel selection is used to select a channel without tuning to that channel. For example, a user can select a channel as described above for recording at some future time. In this case, the digital television does not necessarily tune to the selected channel at the time of selection.

This disclosure describes numerous implementations of the invention. However, these implementations are illustrative and not limiting. Additional variations are possible and will be apparent to one of ordinary skill in the appropriate art.

What is claimed is:

- 1. A digital television, comprising:
- a display;
- a tuner including a connection for an externally supplied broadcast signal, where the tuner provides a signal 65 carried on a physical channel selected from the broadcast signal;

- a channel control circuit which derives major and minor channel number sequences from received control signals, where a major and minor channel number sequence indicates a specific channel carried in the broadcast signal;
- a channel processing circuit connected to the channel control circuit, the display, and the tuner, where the channel processing circuit
- determines, when a physical channel indicated at least by the major channel number is digital, a major and minor channel number sequence by displaying a list of channels associated with the physical channel;
- receives a selection of a minor channel from the list, and
- generates a major and minor channel number sequence based thereon.
- The digital television of claim 1, where the received control signals include a major channel number, a delimiter, and a minor channel number.
- 3. The digital television of claim 1, where the received control signals include a major channel number and a menu selection which indicates a minor channel number.
- 4. The digital television of claim 1, where the channel processing circuit comprises a channel look up table which indicates correspondences between major and minor channel number sequences and physical channels.
- 5. The digital television of claim 4, where the channel look up table further indicates correspondences between major and minor channel number sequences and channels encoded in digital signals carried in the broadcast signal.
- The digital television of claim 4, further comprising an integrated keypad for inputting the received control signals.
- 7. The digital television of claim 4, further comprising an input device which includes a keypad for inputting the received control signals.
- 8. A method for selecting a channel in a digital television, 40 comprising:
 - inputting a major channel number which indicates a first physical channel carried on a broadcast signal;
 - determining whether the physical channel is digital;
 - if the physical channel is digital, presenting a list at least of minor channel numbers associated at least with the physical channel;
 - using the list, inputting a minor channel number such that a major and minor channel number sequence can be generated therefrom.
 - 9. The method of claim 1, where the second physical channel is the same as the first physical channel.
 - 10. The method of claim 1, further comprising inputting a completion command to complete selecting a channel.
 - 11. The method of claim 1, further comprising transmitting the major channel number, the delimiter, and the minor channel number to a digital television.
- 12. The method of claim 11, where the major channel number, the delimiter, and the minor channel number are transmitted to the digital television together.
 - 13. The method of claim 1, where the digital signal is a transport stream.
 - 14. The method of claim 13, where a correspondence between the minor channel number and the channel is provided by a virtual channel table carried in the transport stream.

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10 stem for selecting a channel in a digital to

- 15. A method for selecting a channel in a digital television, comprising:
 - receiving a physical channel number sequence which indicates a physical channel which has a corresponding major channel number;
 - identifying the physical channel as analog or digital;
 - when the physical channel is digital, determining a major and minor channel number sequence by displaying a menu listing one or more channels asso-

ciated with the physical channel,

receiving a selection from the menu, where the selection corresponds to a channel which has a corresponding minor channel number, and

generating a major and minor channel number sequence from the major channel number corresponding to the physical channel and the minor channel number corresponding to the selection.

16. The method of claim 15, further comprising tuning to the physical channel corresponding to the major and minor channel number sequence.

17. The method of claim 15, further comprising, when the physical channel is analog, causing a tuner to tune to the physical channel to supply a signal carried on the physical channel to a display.

- 18. A system for selecting a channel in a digital television, comprising:
 - means for receiving a physical channel number sequence which indicates a physical channel which has a corresponding major channel number;
 - means for identifying the physical channel as analog or digital;
 - means for causing a tuner to tune to the physical channel to supply a signal carried on the physical channel to a display when the physical channel is analog;
 - means for determining a major and minor channel number sequence when the physical channel is digital, by displaying a menu listing one or more channels asso-

ciated with the physical channel,

- receiving a selection from the menu, where the selection corresponds to a channel which has a corresponding minor channel number, and
- generating a major and minor channel number sequence from the major channel number corresponding to the physical channel and the minor channel number corresponding to the selection.

* * * * *

EXHIBIT K

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US005285285A

United States Patent [19]

Yamada et al.

[11] Patent Number:

5,285,285

[45] Date of Patent:

Feb. 8, 1994

[54]	METHOD OF CONTROLLING FIRST ITEMS
	THAT REQUIRE PRIOR CRT DISPLAY AND
	SECOND ITEMS THAT REQUIRE NO PRIOR
	DISPLAY

[75] Inventors: Hisafumi Yamada, Tokyo; Mitsumasa Saitoh; Shigeyuki Sano,

both of Kanagawa; Takao Itabashi,

Tokyo, all of Japan

[73] Assignee: Sony Corporation, Tokyo, Japan

[21] Appl. No.: 875,396

[22] Filed: Apr. 29, 1992

[30] Foreign Application Priority Data

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Primary Examiner—Mark R. Powell Assistant Examiner—Chris Grant

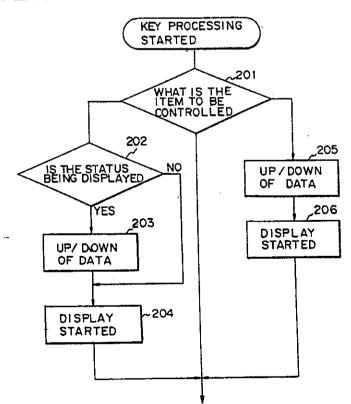
Attorney, Agent, or Firm-Lewis H. Eslinger; Jay H. Maioli

.[57]

ABSTRACT

Items related to the quality of an on-screen image such as brightness, sharpness, chroma, etc. and items related to the audio quality such as bass, treble, balance, etc. in a CRT display, such as a television receiver, are subject to adjustment by a user. These items are originally classified into those in a first class and those in a second class in accordance with the nature of a respective item, that is, whether a user must know the current analog value of the item before he or she adjusts it. When an instruction is input through user's manipulation to adjust the analog value of an item to be controlled, the system determines whether the item belongs to the first class or the second class. If it belongs to the first class, the system first confirms that the item and its actual analog value are displayed on a screen, then permits adjustment of the analog value in response to the instruction, and then displays a new analog value. If it belongs to the second class, the system permits immediate adjustment of its analog value and displays a new analog value.

3 Claims, 3 Drawing Sheets



Sheet 1 of 3

Fig. 1

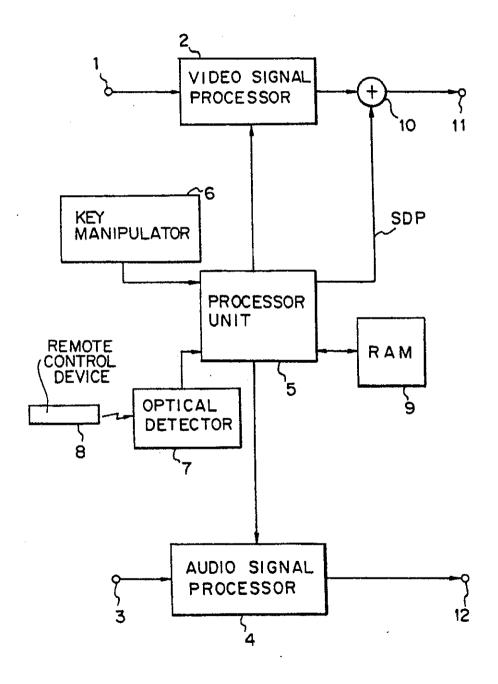
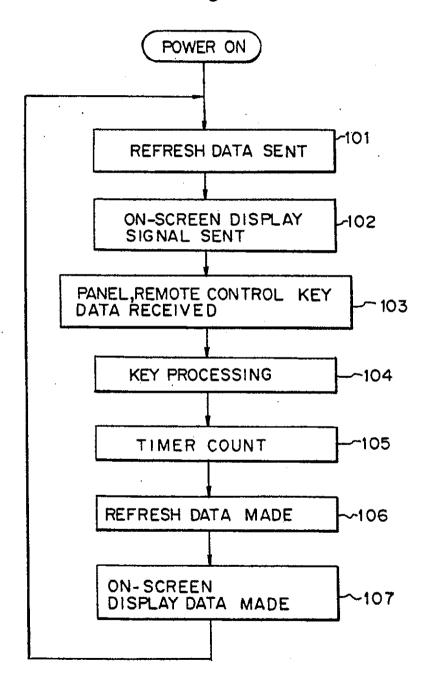


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Fig. 2



EXHIBIT_

Fig. 3

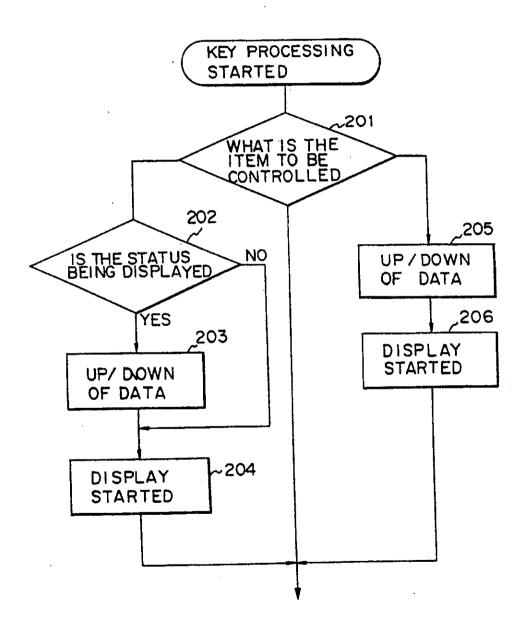


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1

METHOD OF CONTROLLING FIRST ITEMS THAT REQUIRE PRIOR CRT DISPLAY AND SECOND ITEMS THAT REQUIRE NO PRIOR DISPLAY

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a method for displaying a controlled status and, more particularly, to an improvement of display on a screen effected upon adjustment of a CRT display.

2. Description of the Prior Art

A recent type of television receivers is configured to 15 display on its screen the amount of a respective item to be adjusted when a user adjusts the volume, the tone, the hue, the brightness, and so forth. There are, in general, two types of on-screen display shown below.

The first type is such that a current analog value is 20 first displayed on a screen in order to permit a user to select a desired analog value with reference to the current analog value through key manipulation, and a new analog value selected is displayed on the screen.

The second type is such that a new analog value 25 selected by a user through key manipulation is directly displayed on a screen.

In order for a user to control an analog value for control of a CRT display such as a television receiver, he or she needs knowledge on the current status before the intended control for some of such items to be controlled, but need not know it for the other items.

Examples of items for which a user must know the current status, such as identification of the item, its current analog value, and so on, are: brightness, sharpness, phase, chroma, and so on, related to the image display status; and bass, balance, and so on, related to the audio quality.

For such items for which a user must know the current status, the first type on-screen display is necessary. That is, an analog value that has been set heretofore must be displayed before control manipulation.

Examples of items for which a user need not known the current status are: contrast, related to the condition of image display; and volume, related to the audio quality.

For such items for which a user need not know the current status, the second type on-screen display on a screen is desired. That is, it is sufficient that a new analog value selected by a user through key manipulation be directly displayed on the screen

Existing television receivers, however, do not clearly distinguish the use of the above-mentioned types of on-screen display in accordance with the necessity of 55 confirmation of the current status of a respective item to be controlled.

For example, when a user wants to control one of the items: brightness, sharpness, phase and chroma, the current analog value must be displayed on the screen 60 before the control manipulation. Actually, however, this is not done so in some cases. Therefore, the existing television receivers are not always convenient for users.

OBJECT AND SUMMARY OF THE INVENTION

It is therefore an object of the invention to provide a method for displaying a controlled status, which clearly distinguishes the use of the types of on-screen display in 2

accordance with the necessity of confirmation of the current status of a respective item to be controlled.

According to an aspect of the invention, there is provided a method for displaying a controlled status in a system including a manipulating key for adjusting a plurality of items to be controlled, a control unit coupled to the manipulating key for generating a control signal for adjustment, a signal processor responsive to the control signal for controlling a video signal or an audio signal, and a CRT display for simultaneously displaying a video signal from the signal processor and an adjusting value of the control signal on a screen, comprising the steps of:

receiving an instruction signal from the manipulating key and identifying that the item to be controlled is of a first type or a second type;

if the item to be controlled is identified to be of the first type, confirming that a current controlled value is being displayed on the display unit, and then permitting adjustment by the instruction signal; and

if the item to be controlled is identified to be of the second type, permitting adjustment by the instruction signal.

The above, and other, objects, features and advantage of the present invention will become readily apparent from the following detailed description thereof which is to be read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a circuit for discriminating a controlled status and for making an on-screen display signal which can be applied to the present invention;

FIG. 2 is flow chart showing operations of a processor unit; and

FIG. 3 is a flow chart showing operations of the processor unit.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of the invention is explained below with reference to FIGS. 1 to 3. FIG. 1 shows an arrangement of a circuit for discriminating a controlled status and making an on-screen display signal, which can be applied to this invention. In the arrangement of FIG. 1, a video signal is fed to a video signal processor 2 through an input terminal 1, and an audio signal processor 4 through an input terminal 3. The video signal processor 4 and the audio signal processor 4 are controlled by a processor unit 5.

To the processor unit 5 are coupled a key manipulator 6, an optical detector 7, a RAM 9 and so on. When one of various keys provided in the key manipulator 6 is manipulated, a signal corresponding to the key manipulated is made in the key manipulator 6, and it is sent to the processor unit 5. The optical detector 7 receives and decodes a remote control signal from a remote control commander 8, and sends an obtained signal to the processor unit 5.

In response to the signal from the key manipulator 6 or the signal from the optical detector 7, the processor unit 5 identifies the item to be controlled, such as brightness, sharpness and volume, and the control level, i.e., the analog value, for the item to be controlled.

As will be described later, the processor unit 5 classifies the control items into a first control class and a

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second control class, and produces various kinds of control signals, screen display signals SDP, and so on, which are associated with respective classes. Items in the first control class are those for which a user needs knowledge on the current status, that is, the mode, the 5 analog value, and so on, before he or she controls the analog value. Items in the second class are those for which the user need not know the current status before he or she controls the analog value.

If an item to be controlled belongs to the first control 10 class, the processor unit 5 produces character data on identification of the item and its current analog value in the form of an on-screen display signal SDP, and gives the on-screen display signal SDP to an adder 10. The adder 10 superimposes the on-screen display signal SDP 15 supplied from the processor unit 5 on the video signal supplied from the video signal processor 2. A signal obtained by superimposing the on-screen display signal 5 on the video signal is output through a terminal 11 to a CRT display (not shown) and displayed thereon.

After this, in response to the signal indicative of a controlled item and its analog value, which is supplied from the key manipulator 6 or the remote control commander 8 through the optical detector 7, the processor unit 5 produces character data in the form of the 25 on-screen display signal SDP, which indicates the item to be controlled and its new analog value, i.e., the level of the status after adjustment, and supplies the on-screen display signal SDP to the adder 10. Also in response to the signal indicating the item to be controlled and its 30 analog value, which is supplied from the key manipulator 6 or the remote control commander 8 via the optical detector 7, the processor unit 5 produces various kinds of control signals. These control signals are fed to the video signal processor 2, the audio signal processor 4, 35 and so on.

The video signal processor 2 controls the video signal in response to the control signals from the processor unit 5. The video signal after the control is fed to the adder 10. The adder 10 superimposes to the video signal 40 from the video signal processor 2 on the on-screen display signal SDP, which is supplied from the processor unit 5 and consists of character data indicating the item to be controlled and its newly set analog value. A signal obtained by superimposing the on-screen display signal 45 SDP on the video signal is output through the output terminal 11 to a CRT display (not shown). The audio signal processor 4 controls the audio signal in response to the control signals supplied from the processor unit 5. The controlled audio signal is output through a terminal 50 to operations of the processor unit 5, such as receipt of 12 to a speaker (not shown).

If the item to be controlled belongs to the second control class, the processor unit 5 produces various kinds of control signals in response to the signal indicating the item to be controlled and its analog value, which 55 is supplied from the key manipulator 6 or the remote control commander 8 via the optical detector 7. These control signals are fed to the video signal processor 2, the audio signal processor 4, and so on. The video signal processor 2 controls the video signal in response to the 60 one of the following two classes: control signals from the processor unit 5, and the controlled video signal is fed to the adder 10.

After this, in response to the signal indicating the item to be controlled and its analog value, which is supplied from the key manipulator 6 or the remote control 65 commander 8 through the optical detector 7, the processor unit 5 produces character data in the form of the on-screen display signal SDP, which indicates the item

to be controlled and its new analog value, i.e., the level of the status after adjustment, and supplies the on-screen display signal SDP to the adder 10.

The adder 10 superimposes to the video signal from the video signal processor 2 on the on-screen display signal SDP, which is supplied from the processor unit 5 and consists of character data indicating the item to be controlled and its newly set analog value. A signal obtained by superimposing the on-screen display signal SDP on the video signal is output through the output terminal 11 to a CRT display (not shown).

The processor unit 5 performs, once a vertical scanning period, its operations such as receipt of the signal from the key manipulator 6 or the optical detector 7, control of the video signal processor 2 and the audio signal processor 4, output of the on-screen display signal SDP, on-screen display of the item to be controlled and its analog value, and so on. Control by the processor unit 5 is explained below with reference to FIG. 2.

In a condition where the power is supplied, in step 101, refresh data originally set in a slave CPU is transferred from a master CPU which is the processor unit 5 in this embodiment. Control then passes to step 102.

In step 102, the on-screen display signal SDP made on the basis of character data such as letters, symbols, figures, etc. to be displayed on the screen is sent from the processor unit 5 to the adder 10. Control then moves to step 103.

In step 103, a signal made by manipulation in the key manipulator 6 or the optical detector 7 is received. Control then passes to step 104.

In step 104, an item to be controlled and its analog value are defined on the basis of the signal supplied from the key manipulator 6 or the optical detector 7. Control then moves to step 105.

In step 105, time is counted. When a predetermined time has passed, control passes to step 106.

In step 106, refresh data is made. If control data for each item to be controlled, i.e. the analog value, for each item to be controlled has been controlled in the upward or downward direction by the key processing in step 104, new data on the analog value is set for each item to be controlled. Control then goes to step 107. In step 107, the on-screen display signal SDP is produced on the basis of character data such as letters, symbols, figures, and so on, to be displayed on the screen. After this, control returns to step 101.

With reference to FIG. 3, next explanation is directed a signal from the key manipulator 6 or the optical detector 7, control of the video signal processor 2 and the audio signal processor 4, output of the on-screen display signal SDP, on-screen display of an item to be controlled and its analog value, and so on.

In step 201, an item to be controlled and its analog value are determined on the basis of a signal supplied from the key manipulator 6 or the optical detector 7. In this step 201, the item to be controlled is classified into

(1) First control class:

(1-a) Items directly related to the screen status and requiring user's confirmation of the current level of the analog value. Pertinent items are: brightness, aperture, sharpness, phase, chroma, and so forth. Note that the term "phase" indicates the tone of a color while the term "chroma" represents the depth of a color.

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(1-b) Items related to the audio status and requiring display of the current mode for confirmation. Pertinent examples are: bass, treble, balance, and so forth.

(2) Second control class:

This contains items to be controlled for which a user himself determines in an absolute level whether the analog value is adequate or not and for which the user need not confirm the current analog value before he controls it. Pertinent examples are: contrast, volume, 10 and so forth.

Only when an item is determined to belong to the first control class in step 201, characters such as letters, symbols, figures, etc. indicating an item to be controlled and its current analog value are displayed on the screen. 15 After this, control moves to step 202. If the item is determined to belong to the second class, control goes to step 205. If nothing is done in step 201, control moves to the next process.

In step 202, it is determined whether characters such 20 as letters, symbols, figures, etc. indicating an item to be controlled and its current analog value are being displayed on the screen. If they are, control moves to step 203, and if not, control moves to step 204. In step 203, a signal for controlling the analog value is supplied to the 25 processor unit 5 from the key manipulator 6 or the remote control commander 8 through the optical detector 7. In this step 203, on the basis of a control signal output from the processor unit 5, the video signal processor 2 and/or the audio signal processor 4 control(s) 30 the video signal and/or the audio signal in response to an analog value selected for an intended item to be controlled. At the same time, a new analog value after the control is produced in the form of the on-screen display signal SDP. Control then passes to step 204.

In step 204, characters indicating the item to be controlled and its analog value after the control are displayed on the screen on the basis of the on-screen display signal SDP. The display on the screen lasts for a predetermined time, for example, three seconds. Control then passes to the next process.

In step 205, on the basis of a control signal output from the processor unit 5, the video signal processor 2 and/or the audio signal processor 4 control(s) the video signal and/or the audio signal in response to an analog 45 value selected for an intended item to be controlled. At the same time, an analog value after the control is produced in the form of the on-screen display signal SDP. Control then passes to step 206. In step 206, characters indicating the item to be controlled and its new analog 50 value after the control are displayed on the screen on the basis of the on-screen display signal SDP. The display on the screen lasts for a predetermined time, for example, three seconds. Control then moves to the next process.

According to the embodiment, items to be controlled are classified into the first control class, for which a user needs confirmation of the current status, i.e., the current mode, its analog value, and so on, before control of the analog value, and the second control class, for which a user need not confirm the present status. If an item to be controlled belongs to the first control class, its identification and its analog value are once displayed; then a new controlled analog value obtained by controlling the video signal and/or the audio signal is displayed on the screen. If the item belongs to the second control

class, the video signal and/or the audio signal is (are) processed immediately, and a new analog value after the control is displayed on the screen. Therefore, different types of on-screen display can be properly used in accordance with the nature of a respective item to be controlled, i.e., whether confirmation of the current status of the item is necessary or not. The television receiver is thus convenient for a user.

The embodiment has been described as being applied to a television receiver; however, the invention may also be used in any desired display means other than television receivers.

Having described a specific preferred embodiment of the present invention with reference to the accompanying drawings, it is to be understood that the invention is not limited to that precise embodiment, and that various changes and modifications may be effected therein by one skilled in the art without departing from the scope or the spirit of the invention as defined in the appended claims.

What is claimed is:

1. A method for displaying a controlled status in a system including manipulation means for adjusting a plurality of items to be controlled, control means coupled to said manipulation means for generating a control signal for adjustment, signal processing means responsive to said control signal for controlling a video signal or an audio signal, and display means for simultaneously displaying a video signal from said signal processing means and an adjusting value of said control signal on a screen, comprising the steps of:

receiving an instruction signal relating to an item of said plurality of items which is to be controlled from said manipulation means and, in response to said instruction signal:

identifying the item to be controlled; and

classifying said item to be controlled as being of a first type, for which a user needs confirmation of current status, or a second type, for which a user need not confirm the current status; and then,

if said item to be controlled is classified as being of said first type, confirming that a current controlled value is displayed on said display means, and thereafter permitting adjustment by said instruction signal to produce a new controlled value and displaying the new controlled value on said display means; and

if said item to be controlled is classified as being of said second type, permitting adjustment by said instruction signal to produce a new controlled value without prior display of a current controlled value and then displaying the new controlled value on said display means.

2. A method for displaying a controlled status according to claim 1 wherein said item to be controlled is related to a television monitor incorporating a CRT display.

3. A method for displaying a controlled status according to claim 2 wherein said item to be controlled which is classified as being of said first type is one of brightness, aperture, sharpness, phase, chroma, bass, treble, and balance, and said item to be controlled which is classified as being of said second type is one of contrast and volume.

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EXHIBIT L

EXHIBIT ___ PAGE 339



US005212553A

United States Patent [19]

Maruoka

[11]	Patent	Number:
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5,212,553

[45] Date of Patent:

May 18, 1993

[54]	TELEVISION RECEIVER WITH SELECTIVE MENU DISPLAY			
[75]	Inventor:	Kazuhisa Maruoka, Kanagawa, Japan		
[73]	Assignee:	Sony Corporation, Tokyo, Japan		
[21]	Appl. No.:	744,248		
[22]	Filed:	Aug. 13, 1991		
[30]	Foreign	Application Priority Data		
S	ер. 4, 1990 [Л	P] Japan 2-233664		
[58]	Field of Sea	urch 358/22, 183, 188		
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Primary Examiner—John K. Peng Assistant Examiner—John W. Miller Attorney, Agent, or Firm—Lewis H. Eslinger; Jay H. Maioli

57] ABSTRACT

A television receiver with a menu display function has a BS tuner for producing a video signal and a sound signal from a received television signal that is broadcast from a satellite. The television receiver has a microcomputer for adding a menu display signal to the video signal so that menu information can be displayed on a display unit. The menu display signal represents a plurality of menu items in each of selectable menu modes, and the menu items are selectively erasable from the display unit.

4 Claims, 4 Drawing Sheets

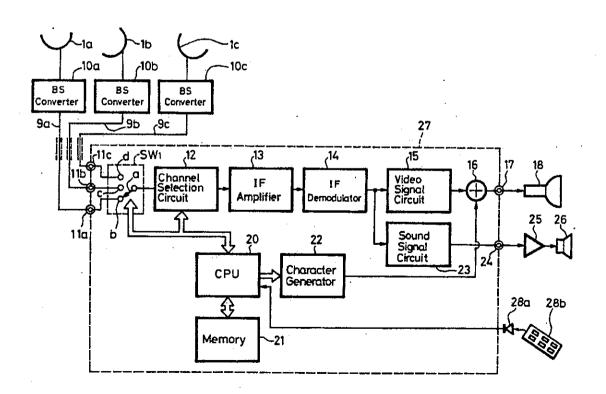


FIG.1

START

ST₁

Push "MENU"

key

ST₂

Select DISPLAY SELECT by "V"

key of remote control unit

ST₃

Push">"key of remote control unit

Push"V"key of remote control unit twice

ST₄

Push">"key

ST₅

remote control unit once

ST₆

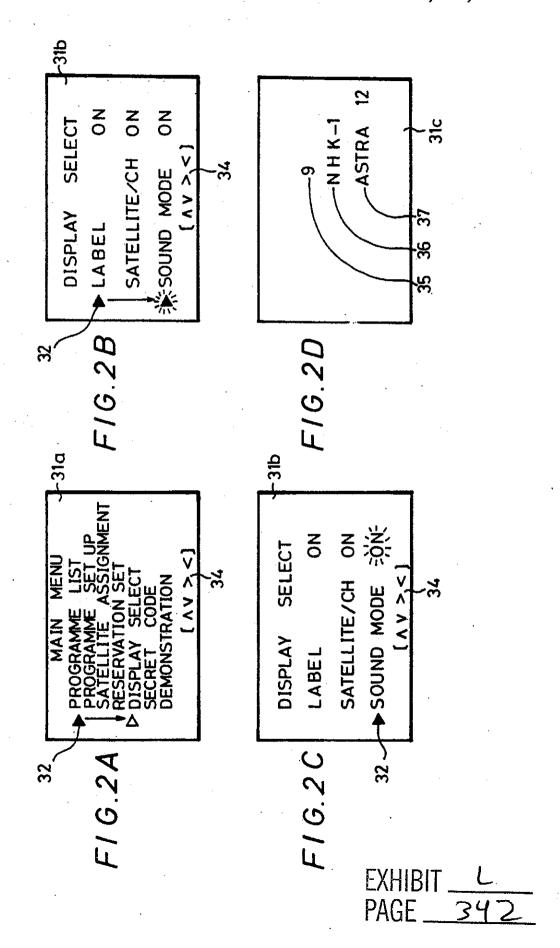
Select ON or OFF by A or V key of remote control unit

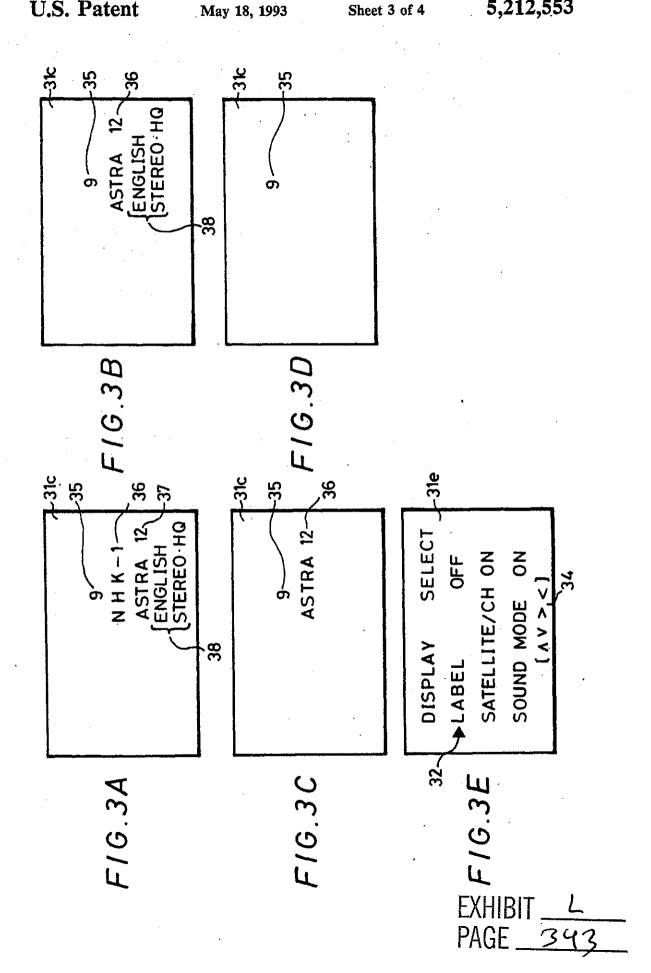
Menu command is displayed

ST7

END

May 18, 1993





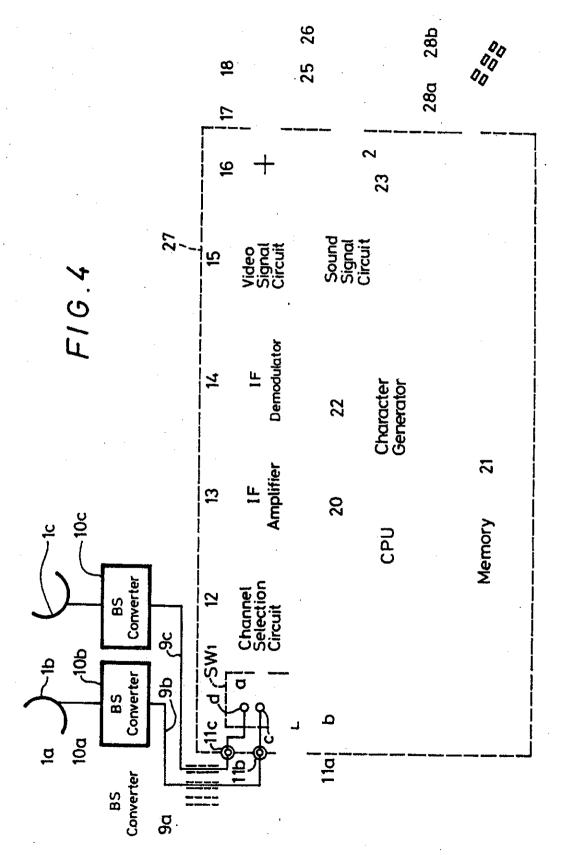


EXHIBIT _____ PAGE _____344 10

2

TELEVISION RECEIVER WITH SELECTIVE MENU DISPLAY

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a television receiver having a menu display function with selective display of menu items.

2. Description of the Prior Art

Television receivers, BS tuners, and some other electronic devices that have recently become available have a menu display function for making themselves easier to handle as well as displaying high-quality images. The menu function enables CRT display units or the like to display menu items for facilitating various settings which would otherwise be rather complex for the user to adjust and establish. Those electronic devices, such as television receivers, which are capable of receiving high-definition broadcasts, and other broadcasts and communications via communication satellites that have newly been launched, however, require more and more difficult settings which may not easily be entered by ordinary users.

The conventional electronic devices which have a ²⁵ menu function display a plurality of standard menu items when in the menu display mode. The displayed standard menu items are permanently established when the electronic devices are designed, and some of the standard menu items may not be necessary for some ³⁰ users.

On the conventional electronic devices, it is possible for the user to turn on or off the entire set of standard menu items. However, the user cannot select a desired one or ones of the standard menu items and then turn on 35 and off the selected standard menu item or items.

When the user wishes to select one of the standard menu items displayed on the display unit, therefore, the user may find the displayed menu information too awkward to deal with.

OBJECTS AND SUMMARY OF THE INVENTION

In view of the aforesaid problems of the conventional television receivers and other electronic devices with a 45 menu function, it is an object of the present invention to provide a television receiver with a menu function or picture in picture function, which television receiver allows the user to select only the menu item or items he needs while leaving other undesirable standard menu 50 items undisplayed.

According to the present invention, there is provided a television receiver comprising circuit means for producing a video signal and a sound signal from a received television signal, display means for displaying an image 55 based on the video signal, and control means for controlling the circuit means to produce the video signal, the control means comprising means for adding to the video signal a menu display signal representing a plurality of selectively erasable menu items.

The control means comprises a character generator for generating characters representing the selectively erasable menu items, and a control unit for controlling the character generator.

The above and other objects, features, and advan-65 tages of the present invention will become apparent from the following description of an illustrative embodiment thereof to be read in conjunction with the

accompanying drawings, in which like reference numerals represent the same or similar objects.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a flowchart of an operation sequence of a television receiver according to the present invention;

FIGS. 2A through 2D are views showing menu items displayed according to the operation sequence shown in FIG. 1:

FIGS. 3A through 3E are views showing the manner in which menu commands are displayed by the television receiver according to the present invention; and

FIG. 4 is a block diagram of the television receiver according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The principles of the present invention are particularly useful when embodied in a television receiver with a BS tuner and BS converters for receiving satellite broadcasts, as shown in FIGS. 1 through 4. First, the arrangement of the television receiver will be described below with reference to FIG. 4.

As shown in FIG. 4, the television receiver includes BS antennas 1a, 1b, 1c in the form of parabolic or planar antennas for receiving dextrorotatory or levorotatory polarized radio waves from a plurality of different satellites. Each of the BS antennas 1a, 1b, 1c has a parabolic reflector, for example, for reflecting a received radio wave in an SHF band, a primary radiating element for receiving the reflected radio wave, and a circular-to-linear polarization converter for converting the dextrorotatory or levorotatory polarized wave into a linearly polarized wave. An RF output in the SHF band from the circular-to-linear polarization converter is supplied to the BS converter 10a, for example. In the BS converter 10a, the supplied RF signal is amplified by an RF amplifier, and the amplified signal is supplied to a mixer through a bandpass filter (BPF). In the mixer, the signal is mixed with a signal from a local oscillator, producing a BS-IF signal in a 1-GHz band, for example. The BS-IF signal from the mixer is then amplified by an intermediate-frequency amplifier, from which the amplified signal is supplied to an output terminal of the BS converter 10a. To the output terminal of the BS converter 10a, there is connected one end of a coaxial cable 9a, the other end of which is connected to an input terminal 11a of a BS tuner 27.

While the BS converter 10a has been described above, the other BS converters 10b, 10c are of the same construction as that of the BS converter 10a.

The BS-IF signals from the BS converters 10a, 10b, 10c are supplied respectively to the input terminals 11a, 11b, 11c of the BS tuner 27. The BS-IF signals are applied to respective fixed contacts b, c, d of an IF terminal selector switch SW1 whose movable contact a is connected to a channel selection circuit 12. The BS-IF signal which is selected by the IF terminal selector switch SW1 is therefore applied to the channel selection circuit 12, by which a desired channel CH is selected from the BS-IF signal. The channel selection circuit 12 includes an RF amplifier, a mixer, and a local oscillator. The mixer and the local oscillator serve to convert the BS-IF signal into an intermediate-frequency signal. The frequency produced by the local oscillator is variable depending on the selected channel.

The intermediate-frequency signal is then supplied from the channel selection circuit 12 to an intermediatefrequency amplifier 13. The intermediate-frequency amplifier 13 has an intermediate-frequency filter for removing unwanted signals other than the intermediate- 5 frequency signal in the selected channel. In the intermediate-frequency amplifier 13, the intermediate-frequency signal is amplified, and passed through an AGC circuit to an amplitude limiter in which it is adjusted to a constant signal level, removing AM noise. Thereafter, 10

the intermediate-frequency signal is frequencydemodulated by a frequency demodulator 14.

The frequency-demodulated signal from the frequency demodulator 14 is supplied to a video signal circuit 15 and a sound signal circuit 23. In the video 15 signal circuit 15, a video signal is extracted from the baseband of the frequency-demodulated signal. The video signal is then supplied through an output terminal 17 to a display unit 18 such as a CRT or the like for displaying an image. In the sound signal circuit 23, a 20 PCM sound signal transmitted by way of differential phase shift keying in the frequency-demodulated signal is demodulated into a sound signal. The sound signal is then supplied through an output terminal 24 and a driver amplifier 25 to a loudspeaker 26, from which the 25 sound is radiated.

The BS tuner 27 has a control unit 20 such as a microcomputer (CPU) for controlling a character generator (CG) 22 which generates messages to be displayed in the form of characters. For example, the control unit 30 20 controls the CG 22 to supply a generated message to one of three primary output terminals, R (red), G (green), B (blue), of the video signal circuit 15, e.g., the output terminal G, so that the message is displayed in G to a photosensor 28a for detecting commands transmitted from a remote control unit 28b, so that the CPU 20 can receive command data from the remote control unit 28b. The CPU 20 also serves to control the channel selection circuit 12. A memory 21 such as a ROM, 40 RAM, or the like is connected to the CPU 20.

Operation of the television receiver shown in FIG. 1 will be described with reference to FIGS. 1, 2A through 2D, and 3A through 3E.

FIG. 1 shows an operation sequence for turning off a 45 sound mode. FIGS. 2A through 2E show displayed menu items by way of example. In FIG. 1, after the power supply of the television receiver is turned on, a menu key on the remote control unit 28b is pushed to display a main menu on the display unit 18 in a first step 50 ST1. At this time, a main menu 31a is displayed on the display unit 18 as shown in FIG. 2A. The main menu 31a displays seven menu modes. The first menu mode represents "PROGRAM LIST", the second menu mode "PROGRAM SETUP", the third menu mode 55 "SATELLITE ASSIGNMENT", the fourth menu mode "RESERVATION SET", the fifth menu mode "DISPLAY SELECT", the sixth menu mode "SE-CRET CODE", and the seventh menu mode "DEM-ONSTRATION".

By way of example, the user pushes a "V" key on the remote control unit 28b, which is represented by a displayed symbol 34, to move a cursor 32 in the main menu to the fifth menu mode, "DISPLAY SELECT", in a second step ST2. Then, with the cursor 32 at the fifth 65 menu item, a ">" key (enter key) on the remote control unit 28b is pushed in a third step ST3, whereupon the display unit 18 displays display select menu information

31b as shown in FIG. 2B. The display select menu information 31b includes items such as "SOUND "SATELLITE/CHANNEL" and MODE". If the television receiver is designed for use in Europe, for example, provision may be made for the user to store six characters, for example, in the memory after having purchased the television receiver. The item "LABEL" indicates the stored characters, and is used to select a predetermined channel. The item "SATEL-LITE/CHANNEL" is used to select a satellite type and channel number. The item "SOUND MODE" is used to select a language such as English, French, or the like, and a quality of reproduced sound. These items are displayed in "ON" state on the display unit 18. In a fourth step ST4, the "V" key on the remote control unit 28b is pushed twice to move the cursor 32 to the item

"SOUND MODE", where the cursor 32 blinks. Then, the ">" key on the remote control unit 28b is pushed once in a fifth step ST5. The cursor 32 no longer blinks, but the displayed item "ON" on the right side of the item "SOUND MODE" starts to blink. If "SOUND MODE" is to be canceled, then "ON" is changed to "OFF" using the "L" or "V" key on the remote control unit 28b. If "SOUND MODE" is not to be canceled, then "ON" remains unchanged. The items "ON" and "OFF" are toggle items. When "SOUND MODE" is canceled, then a selected standard menu command 31c is displayed with "SOUND MODE" erased, as shown in FIG. 2D, in a seventh step ST7. The number "9" displayed in the standard menu command 31c represents a program number 35, the item "NHK-1" a label 36, and the item "ASTRA 12" a satellite type and channel number 37.

The user stores the number of a preferred channel in color on the display unit 18. The CPU 20 is connected 35 the program number 35, and the program number 35 is used for the user to have a clue in receiving the channel. If all the items "LABEL", "SATELLITE/CHAN-NEL", "SOUND MODE" in the menu information shown in FIG. 2B are "ON", then the displayed standard menu command 31c becomes displayed standard men command 31c as shown in FIG. 3A, displaying all the program number 35, the label 36, the satellite type and channel number 37, and also a sound mode 38. Conversely, if all the items "LABEL", "SATELLITE/ CHANNEL", "SOUND MODE" in the menu information shown in FIG. 2B are "OFF", then only the program number 35 is displayed as shown in FIG. 3D, erasing the label 36, the satellite type and channel number 37, and the sound mode 38.

> Other menu commands will be described below with reference to FIGS. 3B, 3C, and 3E. If the label is to be erased, the cursor is moved to "LABEL" as shown in FIG. 3E. Then, the ">" key on the remote control unit 28b is pushed to blink "ON" on the right of "LABEL", and then the "A" key on the remote control unit 28b is pushed to select "OFF", whereupon a menu command with the label 36 erased is displayed as shown in FIG. 3B. FIG. 3C shows a menu command with the label and the sound mode erased.

> Since one or more of the displayed menu items can be selected and selectively be displayed and erased. Therefore, only those menu items which are used to change channels, for example, can be selected and displayed for a simplified displayed menu command. The displayed menu command is easy for the user to see and deal with because unwanted menu items may be omitted.

> While the menu mode "DISPLAY SELECT" has been described above, the other menu modes such as

"SATELLITE ASSIGNMENT" may similarly be selected and processed.

Having described a preferred embodiment of the invention with reference to the accompanying drawings, it is to be understood that the invention is not limited to that precise embodiment and that various changes and modifications can be effected by one skilled in the art without departing from the spirit or scope of the invention as defined in the appended 10 said menu items include menu items representing a teleclaims.

What is claimed is:

1. A television receiver comprising:

circuit means for receiving a television signal and 15 producing a video signal and a sound signal from said received television signal;

display means for displaying an image based on said video signal; and

control means for controlling said circuit means, said control means comprising means for adding to said video signal a menu display signal representing a plurality of menu items and for selectively deleting said items under the direction of a user of the apparatus, whereby all or only selected ones of said menu items can be displayed on said displayed means.

2. A television receiver according to claim 1 wherein vision channel and a sound mode.

3. A television receiver according to claim 1 wherein said circuit means includes a BS receiver for receiving said television signal broadcast from satellite.

4. A television receiver according to claim 1 wherein said control means comprises a character generator for generating characters representing said menu items and said control means controls said character generator.

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EXHIBIT M

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US005168362A

United States Patent [19]

Yoshida

[11]	Patent	Number:
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5,168,362

[45] Date of Patent:

Dec. 1, 1992

[54]	APPARATUS FOR DISPLAYING STANDARD ASPECT RATIO TELEVISION SIGNAL ON WIDE ASPECT RATIO DISPLAY SCREEN
[75]	Inventor: Chisato Yoshida, Saitama, Japan
[73]	Assignee: Sony Corporation, Tokyo, Japan
[21]	Appl. No.: 691,817
[22]	Filed: Apr. 26, 1991
[30]	Foreign Application Priority Data
M	ay 1, 1990 [JP] Japan 2-111739
	Int, Cl. ⁵ H04N 5/16; H04N 5/18 U.S. Cl 358/171; 358/172;
-	358/34; 358/140 Field of Search
[50]	358/141, 142, 22, 183, 171–174, 176, 178, 168–169, 188, 180, 181, 34
[56]	References Cited
	U.S. PATENT DOCUMENTS

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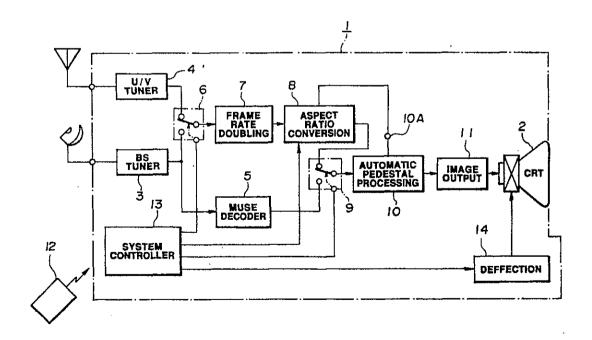
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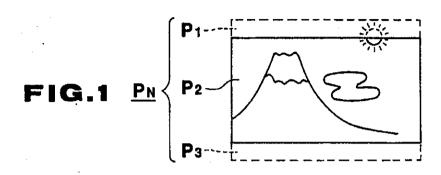
Primary Examiner—James J. Groody
Assistant Examiner—Michael H. Lee
Attorney, Agent, or Firm—Lewis H. Eslinger; Jay H.
Maioli

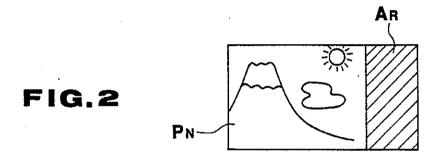
[57] ABSTRACT

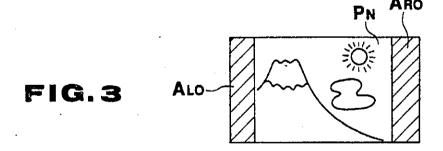
An image display apparatus includes an automatic pedestal processing circuit for detecting the minimum signal level of the input video signal for controlling the signal level of the video signal on the basis of the results of the detection. A control section is provided for activating the automatic pedestal processing circuit during the effective display period for the input video signals to prevent malfunction of the automatic pedestal processing section and to display an image with superior picture quality.

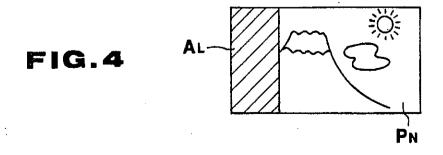
6 Claims, 10 Drawing Sheets











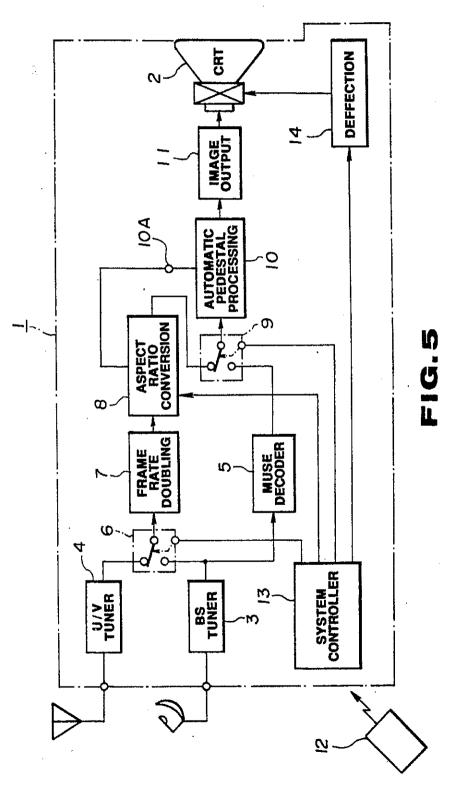


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PAGE <u>351</u>

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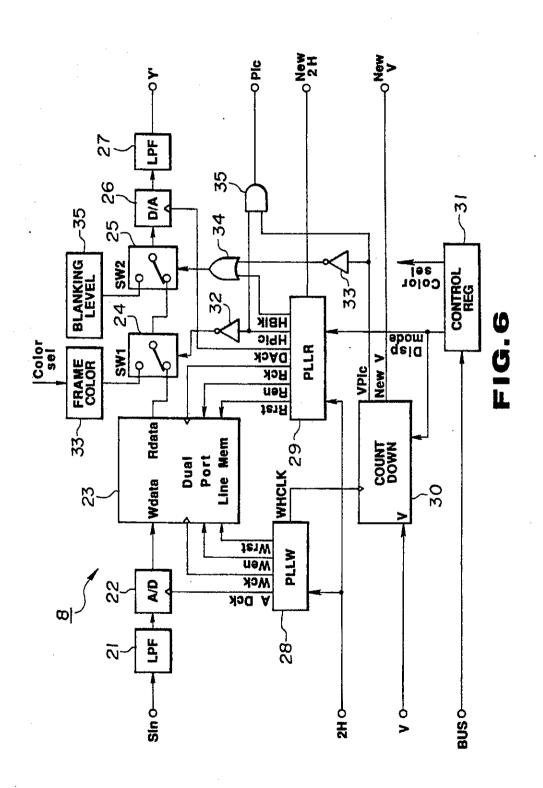
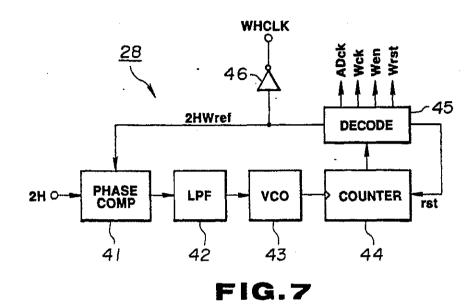
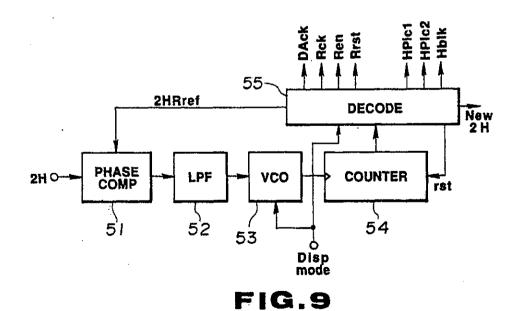
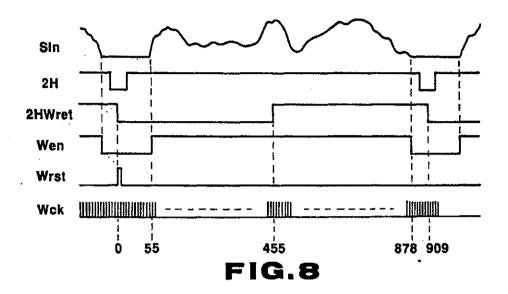


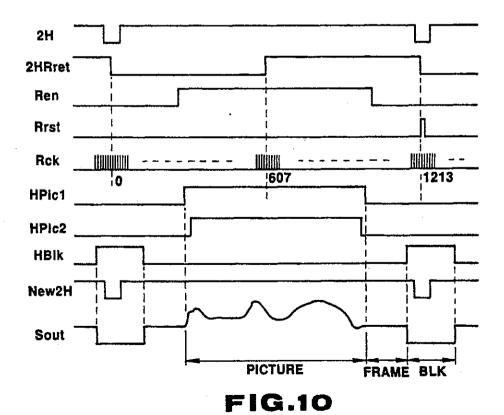
EXHIBIT M PAGE 352





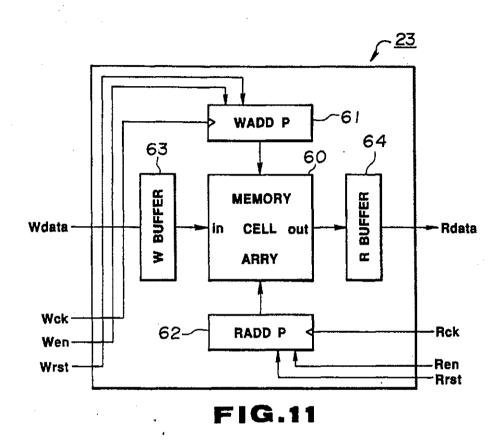
U.S. Patent





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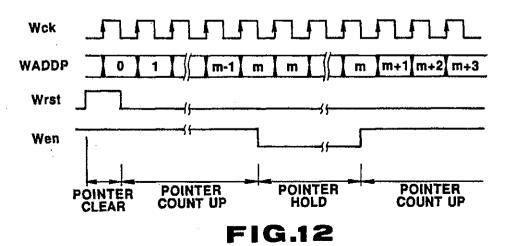
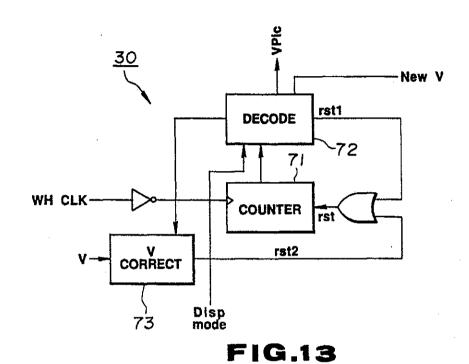
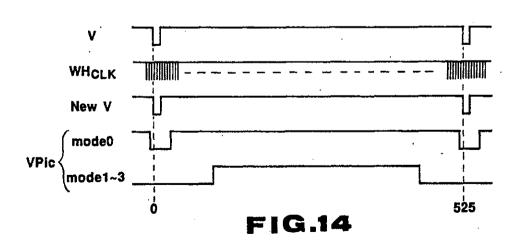
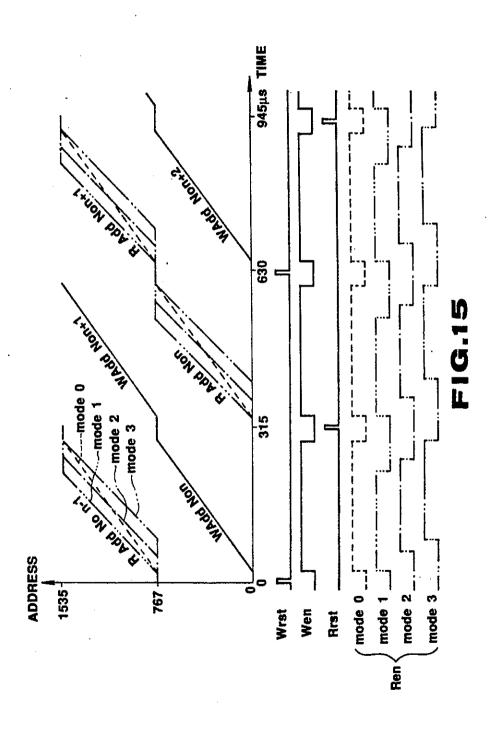


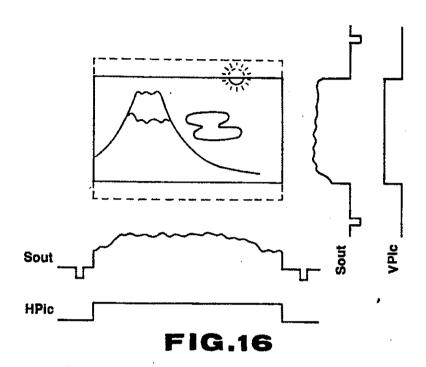
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PAGE 355

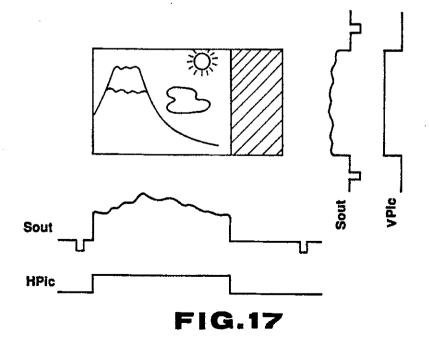


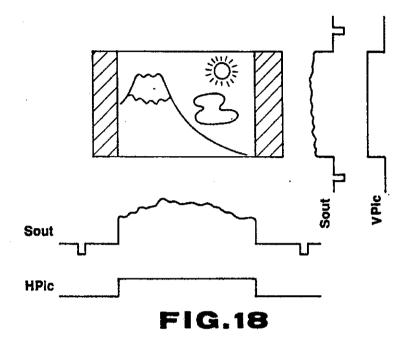


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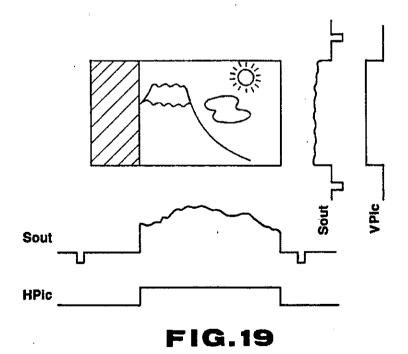


EXHIBIT <u>M</u> PAGE <u>359</u>

APPARATUS FOR DISPLAYING STANDARD ASPECT RATIO TELEVISION SIGNAL ON WIDE ASPECT RATIO DISPLAY SCREEN

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to an image display apparatus provided with an automatic pedestal processing section for detecting the minimum signal level of input video signals and controlling the signal level of the video signals on the basis of the detected results. The present invention may be applied to, for example, an image display apparatus, such as a television receiver having display means in the form of a display raster or screen 15 having a wide aspect ratio.

2. Description of the Prior Art

An image display apparatus, such as a television receiver, adapted for displaying an image by image signals or video signals by on a display means such as a Braun tube or liquid crystal display, has been known widely. With such image display apparatus, an automatic pedestal processing section for detecting the minimum signal level of the input video signals and controlling the signal level of the video signals on the basis of the detected results is provided in the image signal processing system for displaying an image with excellent picture quality by effective exploitation of the dynamic range of the display means.

Meanwhile, with the present television broadcasting 30 system, the display screen has an aspect ratio of 4:3. In a second generation extended definition TV (EDTV), scheduled to be practiced in future, or a high quality television broadcasting system, such as so-called "high vision" broadcasting system, a widescreen having an 35 aspect ratio of 16:9 is scheduled.

Thus it is estimated that television broadcasting in the future will be made with both the presently adopted standard aspect ratio of 4:3 and the wide aspect ratio of 16:9. For this reason, development of an image display 40 apparatus adapted for displaying images of both types of image signals is proceeding at present.

In such image display apparatus, various display systems such as shown in FIGS. I to 4 are presently proposed as the system for displaying the image of the video signals with the standard aspect ratio of 4:3, using display means for the display screen having a wide aspect ratio of 16:9, as an example.

The present

In the first system, upper and lower regions P_1 and P_3 of an image P_N of image signals having a standard aspect ratio are cut as shown in FIG. 1 to display an image P_3 on the entire display screen having a wide aspect ratio. With this first system, the image is displayed on the display screen of the wide aspect ratio by overscanning in the vertical direction of the screen without med-55 dling with the image signals of the standard aspect ratio.

In the second system, as shown in FIG. 2, a right-hand side region A_R of the display raster of the wide aspect ratio is masked and the image P_N of the image signals of the standard aspect ratio is displayed in the 60 left-hand side region of the display raster of the standard aspect ratio. With the second system, the image signals having the standard aspect ratio are compressed along the time axis to three-fourths in the horizontal direction in conformity to the difference in the aspect ratio relative to the display raster of the wide aspect ratio. Frame signals displaying the right-hand side region A_R by, for example, a black tint, are annexed, and

the image display is made on the display screen of the wide aspect ratio by usual raster scanning.

In the third system, shown in FIG. 3, left- and right-hand side regions A_{LO} and A_{RO} of the display raster having the wide aspect ratio are masked and the image P_{NO} of the image signals having the standard aspect ratio is displayed at the center of the display screen of the wide aspect ratio. With this third system, image signals of the standard aspect ratio are compressed along the time base to three-fourths in the horizontal direction, in conformity to the difference in aspect ratio relative to the display screen of the wide aspect ratio. Frame signals associated with the left- and right-hand side regions A_{LO} and A_{RO} are affixed and display is made on the display screen of the wide aspect ratio by usual raster scanning.

In the fourth system, shown in FIG. 4, a left-hand side region A_L of the display screen having the wide aspect ratio is masked, and the image P_N of the image signals of the standard aspect ratio is displayed on the right-hand side of the display screen having the wide aspect ratio. With this fourth system, the image signals of the standard aspect ratio are compressed along the time base to three-fourths in the horizontal direction, in conformity to the difference in the aspect ratio relative to the display screen of the wide aspect ratio. Masking signals associated with the left-hand side region A_L are affixed and display is made on the display screen of the wide aspect ratio by the usual raster scanning.

Meanwhile, with the image display apparatus, adapted for displaying the image of the wide aspect ratio and the image of the standard aspect ratio by display means consisting of the display screen having the wide aspect ratio, a problem is raised in that, when an automatic pedestal processing section is provided for improving the picture quality of the displayed image, the masking signal having the signal level within the range of level detection by the automatic pedestal processing section is erroneously detected as being of the black level, so that the automatic pedestal processing section is erroneously actuated and hence it becomes impossible to make image display in such a manner as to take advantage effectively of the dynamic range of the display means.

OBJECT AND SUMMARY OF THE INVENTION

The present invention has been made in view of the above status of the art. A principal object of the present invention is to provide an image display apparatus adapted for displaying an image of the wide aspect ratio and an image of the standard aspect ratio by display means consisting of the display screen of the wide aspect ratio, in which mistaken actuation of the automatic pedestal processing section may be prevented and an image display may be made in such a manner as to take advantage of the dynamic range of the display effectively.

According to the present invention, the automatic pedestal processing section, controlled in operation by a control section, is operated only during the effective display period for input image signals so as to detect the minimum signal level of the input image signals to control the signal level of the image signals on the basis of the detected results. In this manner, with the image display apparatus according to the present invention, mistaken operations of the automatic pedestal processing section due to detection of signals occurring during

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the ineffective display period other than the effective display period may be eliminated and the dynamic range of the display means may be effectively exploited to enable image display with the desired excellent picture quality.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic front view showing an image displayed in the first system according to which upper and lower regions of the image by the image signals 10 with the standard aspect ratio are cut and the image display is made on the overall display screen having the wide aspect ratio.

FIG. 2 is a schematic front view showing an image displayed in the second system according to which a 15 right-hand side region of the display screen having a wide aspect ratio is masked and the image of the image signals with the standard aspect ratio is displayed on the left-hand side region of the display screen having the wide aspect ratio.

FIG. 3 is a schematic front view showing an image displayed in the third system according to which left-and right-hand side regions of the display screen having a wide aspect ratio are masked and the image of the image signals with the standard aspect ratio is displayed 25 at the center of the display screen having the wide aspect ratio.

FIG. 4 is a schematic front view showing an image displayed in the fourth system according to which a left-hand side region of the display screen having the 30 wide aspect ratio is masked and the image of the image signals with the standard aspect ratio is displayed on the right-hand side region of the display screen having the wide aspect ratio.

FIG. 5 is a block diagram showing an arrangement of 35 an image display apparatus according to the present invention.

FIG. 6 is a block diagram showing an arrangement of an aspect ratio converting circuit of the image display apparatus shown in FIG. 5.

FIG. 7 is a block diagram showing an arrangement of a write clock generating circuit of the aspect ratio converting circuit shown in FIG. 6.

FIG. 8 is a time chart for illustrating the operation of the write clock generating circuit shown in FIG. 7.

FIG. 9 is a block diagram showing an arrangement of a readout clock generating circuit of the aspect ratio converting circuit shown in FIG. 6.

FIG. 10 is a time chart for illustrating the operation of the readout clock generating circuit shown in FIG. 9. 50

FIG. 11 is a block diagram showing an arrangement of a line memory of the aspect ratio converting circuit shown in FIG. 6.

FIG. 12 is a time chart for illustrating the operation of data reading from the line memory shown in FIG. 11. 55

FIG. 13 is a block diagram showing an arrangement of a countdown circuit of the aspect ratio converting circuit shown in FIG. 6.

FIG. 14 is a time chart for illustrating the operation of the countdown circuit shown in FIG. 13.

FIG. 15 is a time chart for illustrating the operation of the aspect ratio converting circuit of FIG. 6 in each of the display modes.

FIG. 16 is a schematic waveform diagram for explaining the position of generation of a control signal 65 used for actuating an automatic pedestal processing circuit during the period of effective display of the image signals in the display mode for displaying the

image on the overall display screen having the wide aspect ratio by cutting upper and lower regions of the image of the image signals with the standard aspect ratio.

FIG. 17 is a schematic waveform diagram for explaining the position of generation of a control signal used for actuating an automatic pedestal processing circuit during the period of effective display of the image signals in the display mode for displaying the image of the image signals of the standard aspect ratio a left-hand region of the display screen of the wide aspect ratio by making the right-hand side region of the display screen with the wide aspect ratio.

FIG. 18 is a schematic waveform diagram for explaining the position of occurrence of a control signal used for actuating an automatic pedestal processing circuit during the period of effective display of the image signals in the display mode for displaying the image of the image signals with the standard aspect ratio in the center of the display screen having the wide aspect ratio by masking the left- and right-hand side reigons of the display screen having the wide aspect ratio.

FIG. 19 is a schematic waveform diagram for explaining the position of occurrence of a control signal used for actuating an automatic pedestal processing circuit during the period of effective display of the image signals in the display mode for displaying the image of the image signals with the standard aspect ratio in the right-hand side region of the display screen having the standard aspect ratio by masking the left-hand side region of the display screen having the wide aspect ratio.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT

By referring to the drawings, an illustrative preferred embodiment of the image display apparatus according to the present invention will be explained in detail.

In an image display apparatus 1, shown in FIG. 5, the present invention is applied to a high definition television receiver displaying an image by a picture tube 2 having a display raster of a wider aspect ratio of 16:9.

The image display apparatus 1 has a broadcast satel-45 lite (BS) tuner circuit 3 for transmitting and receiving signals of satellite broadcasting and a UHF/VHF (U/V) tuner circuit 4 for transmitting and receiving ground waves.

The MUSE signals, obtained as the reception output by the BS tuner circuit 3 of the high definition broadcasting, are supplied to a MUSE decoding circuit 5 and thereby decoded into high quality video signal.

The video signals of the NTSC system, obtained as the reception output by the BS tuner circuit 3 or the U/V tuner circuit 4, are supplied to a frame rate doubling conversion circuit 7 by means of an input changeover switch circuit 6. The frame rate doubling conversion circuit 7 processes the NTSC system video signals from the BS tuner circuit 3 or the U/V tuner circuit 4 by frame rate doubling conversion whereby the interlaced scanning mode video signals are converted into sequential scanning mode video signals or double-rate video signals. The double-rate video signals, obtained by the frame rate doubling conversion circuit 7, are supplied to an aspect ratio converting circuit 8. This aspect ratio converting circuit 8 processes the doublerate video signals from the frame rate doubling conversion circuit 7 by aspect ratio conversion whereby the

image having a standard aspect ratio of 4:3 according to the NTSC system is to be displayed on the display screen of the picture tube 2 in accordance with any of the above mentioned first to fourth display systems. The circuit 8 also generates a control signal for indicating the effective display period of the image signals in each of the above display systems by, for example, a logical "H" level.

The high quality video signals, obtained upon decoding the MUSE signals by the MUSE decoding circuit 5, 10 and the double-rate video signals, processed by the aspect ratio converting circuit 8 by aspect ratio conversion, are selectively supplied to an automatic pedestal processing circuit 10 by means of a signal changeover switch circuit 9. The automatic pedestal processing 15 circuit 10 remains in operation during the time period when the control signal of the logical "H" level is supplied to its control input terminal 10A to detect the minimum signal level of the input video signals and processes the input video signals by automatically con- 20 memory 23, and reset control signals W_{rst} for initializing trolling the signal level of the video signals in their entirety on the basis of the detected signal level. The video signals, the signal level of which has been controlled automatically by the automatic pedestal processmeans of an image output circuit 11 for displaying the image on a display screen of the picture tube 2 having the wider aspect ratio of 16:9.

The image display apparatus 1 includes a system controller 13 for accepting the control input by a remote 30 controller 12 to execute various control operations, such as switching control of the switching circuits 6 and 9, operational control of the aspect ratio converting circuit 8 and deflection angle switching control of the

The aspect ratio converting circuit 8 of the image display apparatus 1 of the present embodiment is constructed as shown for example in FIG. 6.

Thus, as shown in FIG. 6, the aspect ratio converting circuit 8 includes an analog/digital converter 22 for 40 digitizing the input video signals, that are bandwidthlimited by a low-pass filter 21, a dual-port line memory 23 for processing the video data digitized by A/D converter 22 by time-base compression, a frame data annexing circuit 24 for annexing frame data to the video data 45 read out from line memory 23, a blanking data annexing circuit 25 for annexing blanking data to the video data to which the frame data have been annexed by the frame data annexing circuit 24, a digital-analog converter 26 for converting the video data, to which the 50 blanking data have been annexed by the blanking data annexing circuit 25, into corresponding analog data and outputting the resulting analog data by means of a lowpass filter 27, a write clock generating circuit 28 for generating the video data writing timing to line memory 55 23, a readout clock generating circuit 29 for generating the video data readout timing from line memory 23, and a count-down circuit 30 for generating the timing necessary for vertical image processing.

The write clock generating circuit 28 is a PLL circuit 60 for forming 8 fsc reference signals necessary for A/D conversion or writing in the memory, and is constituted by a phase comparator 41, to which the double-rate horizontal sync signals 2H, formed in the frame rate doubling conversion circuit 7, are supplied as the refer- 65 ence signals, a voltage controlled oscillator 43, to which an output of phase comparison by the phase comparator 41 is supplied as the control signal by means of a low-

pass filter 42, a counter circuit 44 counting the oscillation output of the voltage controlled oscillator 43, and a decoding circuit 45 decoding the count output from the counter circuit 44, as shown for example in FIG. 7.

In the write clock generating circuit 28, a signal having a frequency of approximately 28 MHz, or 910 times the frequency of the horizontal sync signals 2H, is generated by the voltage-controlled oscillator 43 and frequency-divided by 1/910 by the counter circuit 44 and the decoder circuit 45 to form a comparison signal 2HWm, which comparison signal 2HWm/is phase-compared in the phase comparator 41 with the horizontal sync signal 2H, in a closed loop configuration. The count output from the counter circuit 44 is decoded by the decoding circuit 45 to produce clock signals ADck for providing an operational timing of the A/D converter 22, write clocks Wck for providing the video data write timing to the line memory 23, write control signals Wen for delimiting the write domain in the line the write address pointer in the line memory 23. The waveforms of these signals are shown in FIG. 8.

The readout clock generating circuit 29 is a PLL circuit for forming reference signals necessary to pering circuit 10, are supplied to the picture tube 2 by 25 form the readout operation from the memory, and is adapted for generating the two types of reference signals as a function of the operating modes. As shown for example in FIG. 9, the readout clock generating circuit 29 is constituted by a phase comparator 51, to which the double-rate horizontal synchronizing signals 2H, formed in the above mentioned frame rate doubling conversion circuit 7, are supplied as the reference signals, a voltage controlled oscillator 53, to which the phase comparison output from the phase comparator 51 is supplied as the control signal by means of a low-pass filter 52, a counting circuit 54 for counting the oscillation output of the voltage controlled oscillator 53 and a decoding circuit 55 for decoding the count output of the counting circuit 54.

In the readout clock generating circuit 29, the operation of each of the voltage controlled oscillators 53 and the decoding circuit 55 is switched by control data in conformity to the display mode supplied from the system controller 13 to the control register 31. Thus, on reception of control data of the display mode according to the above mentioned first display system (mode 0 control data), the readout clock generating circuit 29 constitutes a PLL circuit generating reference signals having the frequency of 8 fsc, similar to the above mentioned write clock generating circuit 28 and, on reception of control data of the display mode according to the above mentioned second to fourth display systems (mode 1 to 3 control data), the readout clock generating circuit 29 constitutes a PLL circuit generating reference signals having the frequency of 8 fsc, similar to the write clock generating circuit 28. Likewise, on reception of control data according to the above mentioned first to fourth display systems (mode 1 to 3 control

reference frequency 2H, or about 38 MHz. Referring to FIG. 10, the decoder circuit 55 decodes the count output from the counter circuit 54 to generate clock signals DAck for providing the operational timing for the D/A converter 26, readout clocks R_{ck} for providing the readout timing for reading out image data from line memory 23, write control signals Ren for de-

data), the circuit 29 constitutes a PLL circuit generating

reference signals having the 4/3-fold frequency, that is the frequency equal to 1213 times the above mentioned

limiting the readout domain of the line memory 23, reset control signals R_{rst} for initializing a readout address pointer in the line memory 23, control signals HP_{lc} necessary for frame data addition and automatic pedestal processing, control signals HB_{lk} necessary for blanking data addition, and new horizontal synchronizing signals NEW 2 H.

The timing of generation of each of the control signals R_{en} , R_{rsi} and HP_{lc} , generated by the readout clock generating circuit 29, is switched by control data supplied to the control register 31. Thus the signals R_{en} , R_{rsi} and HP_{lc} are generated at the timings conforming to the display position in the image display screen in accordance with the display modes (modes 0 to 3).

FIG. 10 shows the case of the display mode according to the above mentioned third system (mode 2).

It is noted that stabilized timing generation may be realized with the readout clock generating circuit 29 even when no signals are received during broadcast reception and no reference signals 2 H are received, because the voltage controlled oscillator 53 may continue its operation in the free-running state.

Meanwhile, the line memory 23 of FIG. 6 is a FIFO type line memory for asynchronous data writing and reading and includes, as shown in FIG. 11, a memory cell array 60, a write address pointer 61 for applying a write address to the memory cell array and a readout address pointer 62 for applying a readout address to the memory cell array 60. Input data W_{data} entered by means of an input buffer 63 are written in a memory cell of the memory cell array 60 which is designated by the write address applied from the write address pointer 61, while output data R_{data} read out from a memory cell of the memory cell array 60 designated by the readout address applied from the readout address pointer 62 are outputted at an output buffer 64.

In the line memory 23, the write clock signals W_{ck} and the various control signals W_{en} and W_{rsi} , generated by the write clock generating circuit 28, are supplied to the write address pointer 61, while the readout clock signals R_{ck} and the control signals R_{en} and R_{rsi} , generated by the readout clock generating circuit 29, are supplied to the readout address pointer 62. To the input buffer 63, image data digitized by the A/D converter 22 are supplied as the above mentioned input data W_{data} .

The input data W_{data} , entered to the memory cell array 60 by means of the input buffer 63, are written by the write address pointer 61, during the period when the write control signal W_{en} is at the logical high level, in a 50 memory cell of the memory cell array 60 which is accessed in synchronism with the rising of the write clock signal W_{ck} .

Referring to FIG. 12, the write address pointer 61 is counted up by the write clock signal W_{ck} , during the 55 interval when the write control signal W_{en} is at the logical high level, to access the next address memory cell of the memory cell array 60. On the other hand, when the write control signal W_{en} is at the logical low level, count-up of the write address pointer 61 is inhibited. This causes data writing into the memory cell array 60 to be discontinued. The write control signal W_{en} delimits the data write domain. On the other hand, during the time interval when the reset control signal W_{rsr} is at the logical high level, the write address pointer 65 f1 is initialized in synchronism with the rising of the write clock signal W_{ck} to access the O-address memory cell.

It is noted that the write address pointer 61, supplied with the readout clock signals R_{ck} and the control signals R_{en} and R_{rst} , generated by the readout clock generating circuit 29, performs an operation similar to that of the write address pointer 61.

The line memory 23 is capable of performing asynchronous data writing and reading, such that, by setting the frequency of the readout clock signals R_{ck} so as to be equal to 4/3 times that of the write clock signals W_{ck} , the line memory causes the image to be compressed by a factor of $\frac{3}{4}$ in the horizontal direction to realize the image display according to the display modes 1 to 3 of the aforementioned second to fourth display systems. Meanwhile, in the display mode of the first display system (mode 0), the frequency of the write clock signals W_{ck} is set so as to be equal to that of the readout clock signal R_{ck} .

The count-down circuit of FIG. 6 is constituted, as shown for example in FIG. 13, by a counter circuit 71, to which the comparison signal 2 HW_{ref} generated by the write clock generating circuit 28 is supplied as clock signal WH_{clk} by means of an output buffer 46, and a decoder circuit 72 for decoding the count output from the counter circuit 71.

It is noted that the comparison signal 2 HW_{ref} , generated by the write clock generating circuit 28, that is the aforementioned clock signal WH_{clk} , has its rising edge situated at approximately the same position as the double rate horizontal synchronizing signal 2 H generated by the aforementioned frame rate doubling conversion circuit 7 and is synchronized with the horizontal synchronizing signal 2 H, although with a stationary phase error. That is, the clock signal WH_{clk} may be regarded as being similar to the horizontal sync signal 2 H.

The counter circuit 71 in FIG. 13 is reset by a reset control signal rst 2 from a waveform correction circuit 73 to count 525 clock signals WH_{clk}, which number is equal to the number of the double-rate raster scanning lines. The reset control signal rst 2 is generated in the waveform correction circuit 73 by eliminating the jitter component from the vertical sync signal V.

The decoder circuit 72 decodes the count output from counter circuit 71 to output a new vertical synchronizing signal NEWV, and a control signal VP_{ic} as shown in FIG. 14. The control signal VP_{ic} is used for annexing the flanking data and indicates the image domain in the vertical direction by the logically high level.

Meanwhile, the counter circuit 71 is reset by the logical sum of a reset control signal rst 1, generated by the decoder circuit 72, and a reset control signal rst 2, generated from the vertical sync signal V by the waveform correction circuit 73. In this manner, even when the vertical sync signal V has been unable to be detected at the normal position due to, for example, the weak electrical field during broadcast reception, the stable reset control signal rst 1 guarantees correct resetting of the counter circuit 71. In order to provide for stable resetting of the counter circuit 71, the waveform correcting circuit 73 judges the relation between the clock signal WHclk, that is the double-rate horizontal sync signal 2 H, and the vertical synchronizing signal V. If the relation is found to be within a predetermined allowable range in view of the EDTV standards, the reset control signal rst 2 is outputted and, if otherwise, the signal rst 2 is not outputted.

In the count-down circuit 30, of FIG. 6, the signal used as the clock signal for the counter circuit 71 is not the double-rate horizontal synchronizing signal 2 H,

generated by the above-mentioned frame rate doubling conversion circuit 7, but rather the clock signal WHclk generated by the write clock generating circuit 28 from the comparison signal 2 HWres, so that, even when the double-rate horizontal sync signal 2 H is interrupted under the nil-signal state caused by, for example, a weak electrical field during broadcast reception, the clock signal WHcek continues to be output due to the free-running of the voltage-controlled oscillator 43 of the write clock generating circuit 28. Thus the counter circuit 71 10 of FIG. 13 may continue its counting operation to output the vertical synchronizing signals NEWV and the control signals VPic as stable signals.

FIG. 15 shows the relation between the control signal Wen and Wrst, generated by the write clock generating 15 circuit 28, and the control signals Ren and Rest, generated by the readout clock generator 29 for the display modes (modes 0 to 3), and the relation between the addresses of the write address pointer 61 and the readout address pointer 62 within the line memory 23.

In the above described aspect ratio converting circuit 8 of FIG. 6, the dot-sequential mode video signals generated by the frame rate doubling conversion circuit 7, that is, the double-data video signals, are bandwidth limited by the low-pass filter 21 and processed by anti- 25 aliasing processing before being supplied to the A/D converter 22 where the signals are digitized. The digitized video data from the A/D converter 22 are supplied to and written in the line memory 23 in accordance with the write clock signals Wck generated by the 30 write clock generating circuit 28 and the control signals W_{en} and W_{rst} .

Meanwhile, the write control signal Wen, generated by the write clock generating circuit 28, falls to a logical low level during the blanking domain of the input video 35 signal, so that data writing in the line memory 23 is interrupted during this domain and data writing is performed only during the image domain necessary for processing so as to save the storage capacity of the line memory 23. The data of the blanking domain not writ- 40 ten at this time are added at the readout side circuit.

The reset control signal R_{rst}, generated by the readout clock generating circuit 29, adapted for performing readout control of the line memory 23, is generated at a position delayed by one horizontal scanning period with 45 respect to the reset control signal W₁₃₁ generated by the write clock generating circuit 28, thereby preventing collision between the readout address and the write

Since compression in the horizontal direction is not 50 performed with the display mode of the first system mode 0), the readout control signal Ren generated by the readout clock generating circuit 29, is coincident in timing with the write control signal Wen. With the present display mode (mode 0), since the write clock signal, 55 the write clock signal Wck and the readout clock signal R_{ck} are of the same frequency, the video data read out from line memory 23, delayed by 1 H from the data at the write side, are substantially the same as the latter

With the display mode according to the second to fourth systems (modes 1 to 3), video data are read out from the line memory 23 during the domain when the readout control signals Ren associated with the respective display modes are at the logical high level, so that 65 tively. Vertical and horizontal blanking data are affixed the image is displayed at the corresponding position. In these display modes, the frequency of the readout clock signal Rck is four-thirds that of the write clock signal

Wck, so that the image data in the line memory 23 is read out at a rate equal to four-thirds of that at the write side, as a result of which a display image compressed to three-fourths in the horizontal direction is obtained.

The control signal HPic, generated by the readout clock generating circuit 29, is at the logical high level within the region of the image to be displayed in the horizontal direction, that is, within the effective display period, in each of the display modes 0 to 3.

FIG. 16 shows the display state for the display mode 0 wherein upper and lower regions of the image of the standard aspect ratio are cut to display the image on the overall display screen having a wide aspect ratio. FIG. 17 shows the display state in the display mode 1 in which the right-hand side region of the display raster of the wide aspect ratio is masked to display the image of the image signals of the standard aspect ratio on the left-hand side of the display screen of the wide aspect ratio. FIG. 18 shows the display state in the display 20 mode 2 in which left-hand and right-hand side regions of the display raster having the wide aspect ratio are masked and the image of the image signals having the standard aspect ratio is displayed in the middle of the display raster of the wide aspect ratio. Finally, FIG. 19 shows the display state in the display mode 3 in which the left-hand side region of the display raster of the wide aspect ratio is masked and the image of the image signals of the standard aspect ratio is displayed in the right-hand side region of the display raster of the wide aspect ratio.

The control signal HPic from readout clock generating circuit 29 in FIG. 6 is inverted in polarity by inverter 32 so as to be supplied as a changeover control signal to the frame data addition circuit 24. The frame data addition circuit 24 is constituted by a switch circuit which is adapted for selecting the line memory 23 when the switching control signal is at the logical low level, and which is adapted for selecting a frame data output section 33 when the changeover control signal is at the logical high level to affix frame data to those portions of the image data read out from the line memory 23 which are outside the effective image display region.

The control signal VPic, generated by the countdown circuit 30, is at the logical high level within the region of the image to be displayed in the vertical direction, that is, during the effective display period. This display signal VPic has different signal-generating timings between the display mode of the first display system (mode 0) and the display mode of the other display systems (modes 1 to 3).

The above mentioned control signal VP_{ic}, indicating the effective display period in the vertical direction by the logical high level is inverted in polarity by inverter 36, and supplied to an OR gate 34 that performs the logic OR operation between the inverted signal VPic and the control signal HBik from the readout clock generating circuit 29. The logical sum output from this OR gate 34 is supplied to the blanking data affixing circuit 25 as a changeover control signal.

This blanking data affixing circuit 25 is constituted by a switch circuit, which is adapted to select the frame data affixing circuit 24 or the blanking data output section 37 when the changeover control signal is at the logical low level or at the logical high level, respecby the blanking data affixing circuit 25 to the video data, to which the frame data have been affixed by the frame data affixing circuit 24 as described previously.

The output data from the blanking data affixing circuit 26 are converted by the D/A converted 26 into analog signals and processed by a low-pass filter 27 for anti-aliasing so as to be outputted as the image signals of the display modes 0 to 3.

On the other hand, the control signal HP_{Ic}, indicating the horizontal effective display period, formed by the readout clock generating circuit 29, by the logical high level, and the control signal VP_{Ic}, indicating the vertical 10 effective display domain, formed by the countdown circuit 30, by the logical high level, are transmitted to an AND circuit 35, where the AND operation is taken of these two signals. The AND output of the AND gate 35, indicating the effective display domain of the image signal of the display modes 0 to 3 by the logical high level, is supplied to the control input terminal 10A of the automatic pedestal processing circuit 10 as the operation control signal P_{Ic}.

In this manner, the automatic pedestal processing circuit 10 is in operation only during the effective display period in the display modes 0 to 3, so that optimum automatic pedestal processing may continously be made without malfunctions otherwise caused by detection of the signals during the ineffective display period, that is, during the period other than the effective display period

I claim:

1. A display apparatus for displaying image signals contained in input television signals formed of scanning lines with a blank periods and display periods comprising:

receiving means for receiving at least two types of television signals, the aspect ratio of a first type of the television signals being wider than the aspect ratio of a second type of the television signals and having different respective display periods;

display means for displaying said television signals, said display means having an aspect ratio of said first type of the television signals;

aspect ratio converting means for converting said 45 second type of television signals for display on said display means;

detecting means for detecting a predetermined minimum level of image signals in the input television signals;

automatic pedestal processing means for controlling the signal level of said image signals using output

signals of said detecting means; and

control means for determining a display period of the input image signals and controlling said automatic pedestal processing means only within the determined display period of said image signals, wherein said control means generates a window signal so as to pass said image signals to said automatic pedestal processing means only during said determined display period of said image signals.

2. A display apparatus according to claim 1 wherein said control means generates a selecting signal fed to said aspect ratio converting means for selecting one of a number of modes for displaying said second type of television signals on said display means, in a first of said number of modes said second television signal is overscanned in the vertical direction of said display means and in a second of said number of modes the display period of said second television signal is displayed on said display means with frame data.

- 3. A display apparatus according to claim 2 wherein said aspect ratio converting means includes adder means for adding said frame data to said second type of television signals so as to have the same aspect ratio on said display means in said second mode.
- 4. A display apparatus according to claim 2 wherein said first mode creates display signals scanned on a visible display area on said display means and a non-display signal scanned on a non-visible display area thereon, and in which said non-display signal is scanned in upper and lower areas of said visible display area.

5. A display apparatus according to claim 2:

wherein said first type television signal is based on MUSE television format and said second type television signal is based on NTSC television format.

6. A display apparatus according to claim 2: wherein said aspect ratio of said second type television signal is 4:3 and said aspect ratio of said first type television signal is 16:9.

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EXHIBIT N

EXHIBIT <u>N</u> PAGE <u>366</u>



United States Patent [19]

Kamaguchi et al.

Patent Number: [11]

5,539,425

Date of Patent:

Jul. 23, 1996

[54]	DISPLAY	UNIT				
[75]	Inventors:	Yutaka Kamaguchi; Seiichi Nishiyama; Hisao Sakurai, all of Kanagawa, Japan				
[73]	Assignce:	Sony Corporation, Tokyo, Japan				
[21] Appl. No.: 182,540						
[22]	Filed:	iled: Jan. 14, 1994				
Related U.S. Application Data						
[63]	Continuatio	n of Ser. No. 904,091, Jun. 25, 1992, abandoned.				
[30] Foreign Application Priority Data						
Jun.	27, 1991	[JP] Japan 3-183566				
[52]	U.S. Cl Field of S	G09G 3/30 345/77; 348/691; 348/677 earch 348/173, 805, 48/556, 28, 673, 687, 691, 677, 695, 675; 345/63, 147, 77				
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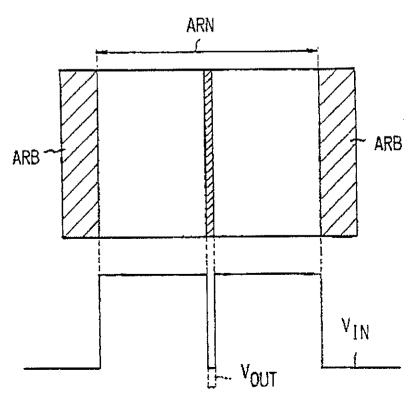
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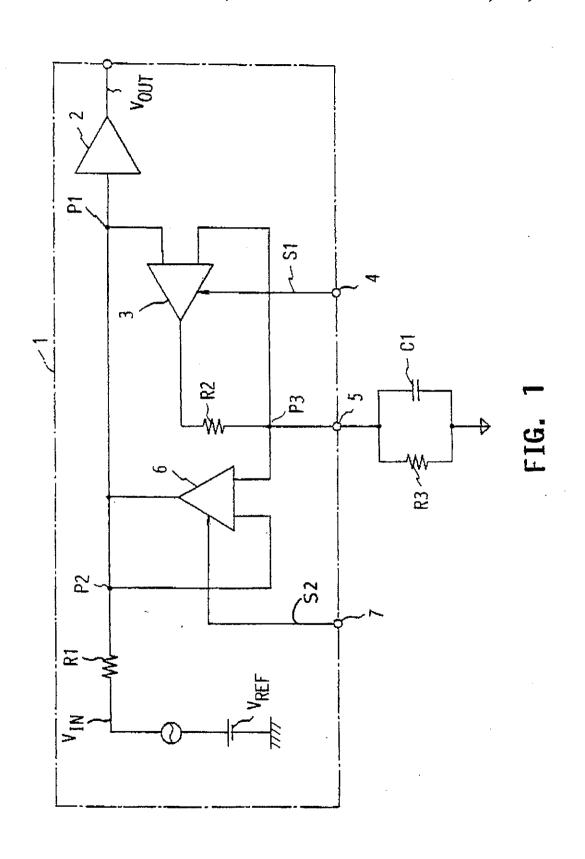
Primary Examiner-Ulysses Weldon Assistant Examiner-Amare Mengistu Attorney, Agent, or Firm-Hill, Steadman & Simpson

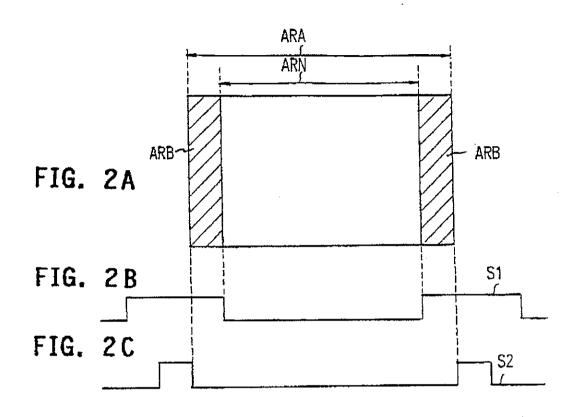
[57] ABSTRACT

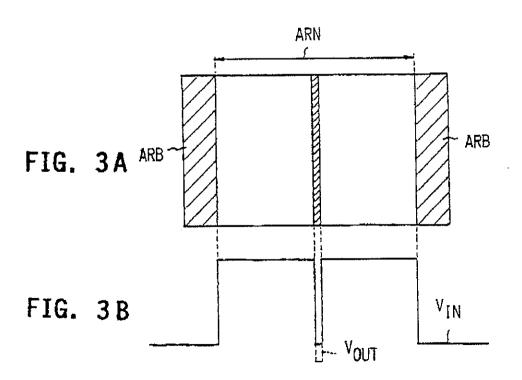
A display unit in which a black level is set to a predetermined level in a first display screen having a first aspect ratio and a black level is set to a predetermined level in a second display screen having a second aspect ratio is provided. A darkest signal of a video signal is detected from an image area corresponding to the second display screen. The darkest signal is lowered to a predetermined level in an image area corresponding to the first display screen. In accordance with the principles of the present invention, the situation where a video signal of the second display screen that is to be lowered will not be lowered can be prevented.

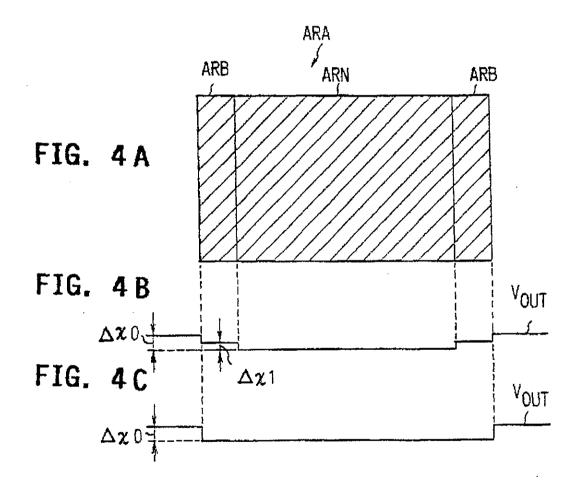
8 Claims, 4 Drawing Sheets











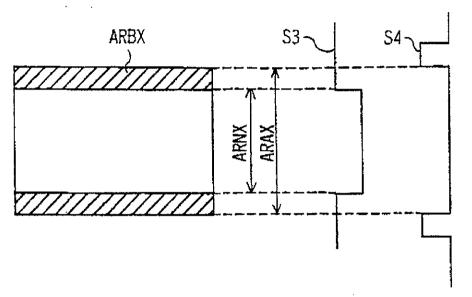


FIG. 5A

FIG. 5B FIG. 5C

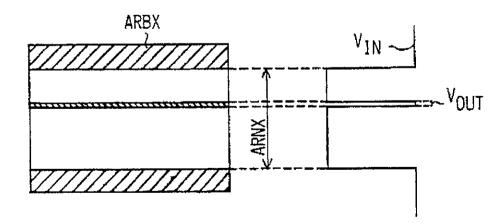


FIG. 6A

FIG. 6B

DISPLAY UNIT

This is a continuation of application Ser. No. 07/904,091 filed Jun. 25, 1992, now abandoned.

BACKGROUND OF THE INVENTION

The present invention relates to a display unit, and is preferable particularly for use on a display unit capable of displaying image screens having a different aspect ratio each 10 on the same screen.

In a television receiver for NTSC system comprising a screen aspect ratio at 4 to 3, in case, for example, a slight black signal is included in an image high in a mean brightness level like a boundary of a bright background and hair, a black portion of the hair is seen to be affoat visually, and hence proposed hitherto is a black signal correction system for enhancing the black portion of the picture by lowering a level of the black signal.

The black signal correction system comprises detecting the darkest signal level in a video signal, lowering the black signal level to a pedestal level to a thicker visibility.

Meanwhile, it is conceivable that such black signal correction system applied not only to the conventional television receiver but also to a high vision receiver for correcting video signals which may ensure images improved still further.

SUMMARY OF THE INVENTION

In view of the foregoing, an object of this invention is to provide to a display unit for use in a television receiver, which is capable of displaying two video signals that are different in display area on the same screen, the display unit being capable of ensuring an image with a quality that is further improved by correcting a black level of the video signal.

The nature, principle and utility of the invention will become more apparent from the following detailed description when read in conjunction with the accompanying drawings in which like parts are designated by like reference numerals or characters.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

FIG. 1 is a circuit connection diagram representing a display unit of one embodiment of the present invention;

FIGS. 2A to 2C are a schematic depiction of a wide aspect display and signal waveform diagrams serving for illustration of a black level detection signal and a blanking pulse signal.

FIGS. 3A and 3B are a schematic depiction of a wide aspect display and a signal waveform diagram serving for illustration of an operation when a video signal that is high in average brightness level is inputted;

FIGS. 4A to 4C are a schematic depiction of a wide aspect display and signal waveform diagrams serving for illustration of an operation when a video signal having a uniform signal level is inputted to a whole image display area;

FIGS. 5A to 5C are a schematic depiction of a conventional aspect display showing a cinema format image and signal waveform diagrams serving for illustration the black 65 level detection signal and the blanking pulse signal in a second embodiment of the present invention; and

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FIGS. 6A and 6B are a schematic depiction of a conventional aspect display and a signal waveform diagram serving for illustration the picture corresponding to an NTSC system in the second embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In order to solve the such problem described above, in a display unit as shown schematically in FIG. 2a for displaying, in a first display screen ARA having a first aspect ratio at 16 to 9, a second display screen ARN having a second aspect ratio at 4 to 3 with a vertical screen length substantially the same as a length of the first display screen, and a horizontal screen length shorter than the first display screen length, displaying an image of a black level in an extra area ARB of the second display screen ARN, a first aspect of the invention comprises signal level expansion means 6 as shown in FIG. 1 for lowering the darkest signal level in the image overall of the display screen to a predetermined level, when the image is displayed in the first display screen ARA.

Further, in the display unit for displaying, in the first display screen ARA having a first aspect ratio at 16 to 9, the second display screen ARN having a second aspect ratio at 4 to 3 with a vertical screen length substantially the same as a length of the first display screen, and a horizontal screen length shorter than the first display screen length, displaying an image of a black level in the extra area ARB of the second display screen ARN, a second aspect of the invention comprises signal level detection means 3 for detecting the darkest signal level in the image only in the second display screen ARN excepting the black-framed screen ARB, when the image is displayed in the second display screen ARN, and signal level expansion means 6 for lowering the signal level to a predetermined level according to a detected result of the signal level detection means 3.

According to the first aspect of the invention, when an image is displayed in the first display screen ARA, the signal level expansion means 6 lowers a black signal of the image displayed in the first display screen ARA from a black level to outputting, therefore in case images of a signal level are inputted to the second display screen ARN and the extra area ARB, a probability of a boundary of the areas being sensed visually can effectively be avoided.

According further to the second aspect of the invention, when an image is displayed in the second display screen ARN of the first display screen ARA, a black signal of a video signal V_{IN} is detected by the signal level detection means 3 only in the second display screen ARN, the detected black signal is lowered from the black level by the signal level expansion means 6, thereby avoiding effectively a probability that the darkest signal level in the second display screen ARN will not be lowered to a predetermined level due to the signal level detection means 6 having detected erroneously the image of the extra area ARB as the darkest.

Preferred embodiments of this invention will be described with reference to the accompanying drawings.

In FIG. 1, a reference numeral 1 indicates a black level correction circuit as a whole, wherein an input video signal V_{IN} superposed on a predetermined reference voltage V_{REF} is outputted through a resistance R1 and an amplification circuit 2 in operational amplifier construction.

The input video signal V_{IN} is supplied to a black level detection circuit 3 in operational amplifier construction which is connected to a connection node P1 whereat the resistance R1 and the amplification circuit 2 are connected.

PAGE _______

The black level detection circuit 3 detects to hold the darkest signal level of the input video signal V_{IN} , when a black level detection signal S1 inputted from a black detection pulse input terminal 4 is low, and stops detection of the darkest signal level of the input video signal V_{IN} , when the 5 black level detection signal S1 is high.

An arrangement is such that the black level detection signal S1 is low in the display area ARN (hereinafter referred to as NTSC image display area) as shown in FIG. 2A on which an NTSC image signal indicated by an aspect ratio at 4 to 3 against the display area ARA (so-called wide screen) of a high vision video signal indicated by an aspect ratio at 16 to 9, and is high in the black-framed areas ARB on opposite ends of the screen (FIG. 2B).

The black-framed area ARB is an area coming outside of the NTSC image display area ARN, and the video signal V_{IN} in the black-framed area ARB has a signal level substantially of the black level.

In this case the black level hold circuit 3 is capable of holding the signal level darkest in the NTSC image display area ARN, signals substantially of the black level in the left and right black-framed areas ARB are detected, thus avoiding a probability of the signal portion darkest in the NTSC image display area ARN not being detected.

An output stage of the black level hold circuit 3 is fed back to an input stage through a resistance R2, and also connected to an external resistance R3 and a capacitor C1 connected in parallel through a pin 5, and thus a predetermined supply voltage is fed thereto.

An arrangement is such that by making a resistance value $_{30}$ and a capacitance of the resistance R3 and the capacitor C1 variable, the black level correction circuit 1 may change a time constant and set a pulse width of the darkest signal that can be detected by the black level hold circuit 3 from the input video signal V_{IN} .

The black level expansion circuit 6 comprises an operational amplifier, loads the input video signal V_{IN} into an input stage from a node P2 whereat the resistance R1 and the amplification circuit 2 are connected, and also loads a voltage at a node P3 whereat the black level hold circuit 3 40 and the pin 5 are connected into the input stage.

While a blanking pulse signal S2 inputted from a blanking pulse input terminal 7 falls, that is, other than a blanking duration, the black level expansion circuit 6 lowers the detected black signal level to a pedestal level (FIG. 2C).

The blanking pulse signal S2 is made to fall covering the whole screen display period.

Thus, when an average brightness level in the NTSC image display area ARN is high and the screen is bright, a signal level of the detected darkest video signal V_{IN} can be lowered to a pedestal level, and even in case the black signal portion is slight, a probability that the black signal portion is seen afloat can be avoided effectively.

Further, a brightness level of the input video signal V_{IN} 55 can be lowered covering the display screen overall, and in case the darkest signal levels in the NTSC image display area ARN and the black-framed area ARB are even, a boundary of the display areas ARA and ARB will not be so sensed.

In the aforementioned construction, when a video signal V_{INN} of the NTSC system is inputted instead of the video signal V_{INN} of a so-called high vision system, the black level hold circuit 3 detects the darkest signal level in the display area ARN according to a black level detection signal S1 65 falling correspondingly to a period of the NTSC image display area ARN.

When an average brightness level of the video signal V_{INW} is high there is less of the black signal, the black level hold circuit 3 does not hold the black signal portion since the darkest signal black level as an area of the black signal in the NTSC image display area ARN (indicated by oblique lines in the NTSC image display area ARN of FIG. 3A) is less than the area of the video signal V_{IN} , the circuit holds a white level signal as the black level.

In this case the black level expansion circuit 6 expands a black signal portion only of the video signal V_{IN} according to the NTSC system for the blanking pulse signal S2 having fallen, thus correcting the video signal V_{IN} to be seen darker than usual.

Then, as in the case of a conventional television receiver for the NTSC system, when operating the black level detection period and the black level expansion period covering the overall display screen area ARA, the black-framed areas ARB on opposite ends of the display area ARA are determined erroneously to be a black level, and thus a probability is that the black signal portion to be expanded essentially will not be expanded.

Thus, from adjusting the black level detection signal S1 so that the black level detection signal S1 does not operate in the black-framed area ARB but operates only in the NTSC image display area ARN, the black level correction circuit 1 is capable of intensifying further a black signal portion of the NTSC system video signal V_{IN} , when the NTSC system image is displayed on a so-called high vision video signal coordinating television receiver.

As shown in FIG. 4A, on the other hand, in case black levels of the video signals V_{IN} inputted correspondingly to the black-framed area ARB and the NTSC image display area ARN are the same, the black level hold circuit 3 operates in the NTSC image display area ARN.

In this case, since the blanking pulse signal S2 is low covering the overall image display area ARA, the black level expansion circuit 6 expands the black signal in the whole image display area ARA including the black-framed area ARB and outputs it from the amplification circuit 2.

A voltage level of an output video signal V_{OUT} becomes to lower by $\Delta \times 0$ (mV) from the black reference level, and a general brightness level of the whole image display area ARA seems to be somewhat low, thereby removing a visual difference in level at a boundary portion of the black-framed area ARB and the image area ARN according to the NTSC system (FIG. 4C).

Meanwhile, when the black level detection signal S1 and the blanking pulse signal S2 are adjusted to fall in the NTSC image display area ARN, the black level expansion circuit 6 operates not to the whole image display area ARA but to the image display area ARN only, therefore a difference in level at $\Delta x1$ (mV) will be sensed visually at a boundary portion of the black-framed area ARB and the image display area ARN according to an offset of the number (mV) to accrue to the black level hold circuit 3 and an offset of the number (mV) to accrue to the black level expansion circuit 6 (FIG. 4B).

Thus, from adjusting the blanking pulse signal S2 to fall so that the black level expansion circuit 6 does not operate in the NTSC image display area ARN central of the screen but operates in the whole image display area ARN according to the NTSC system, when an image of the NTSC system is displayed on a high vision video signal coordinating television receiver, the black level correction circuit 1 is capable of displaying the image in such manner as will not sense visually a boundary portion of the black-framed area ARB

and the image display area ARA according to the NTSC system.

According to the above-described construction, when displaying video signals of the NTSC which is different in aspect ratio on the same screen of a television receiver 5 corresponding to high vision video signals, from detecting a black level of the video signal V_{IN} in the display area ARN corresponding to the video signal of the NTSC system, and expanding the black level within the whole image display area ARA, the black level of the video signal V_{IN} can be detected and expanded in the image area ARN for displaying the image according to the NTSC system, and thus the probability that the black-framed area ARB is detected erroneously as a black level is effectively avoided and the black level of the image area ARN according to the NTSC system is not expanded.

Further, when displaying images in the whole image display area ARA, from expanding the black level covering the whole image display area ARA, a capability of a boundary portion of the black-framed areas ARB on opposite ends of the image area ARA and the NTSC image display area ARN being sensed visually can be avoided effectively.

The above description given for the embodiment has referred to the case where video signals according to the NTSC system which are different in aspect ratio are displayed on a so-called high vision video signal coordinating television receiver, however, the present invention is not necessarily limited thereto, and hence is applicable to a case where video signals which different in aspect ratio from the vision system such as PAL system or the like are displayed.

Further, the above-described embodiment is a exemplified by the case where the black-framed areas ARB are displayed on opposite sides of the NTSC image area ARN, however, the present invention is not necessarily limited thereto, and thus is applicable to a case where the black-framed area ARB is displayed on one side only.

Still further, the above embodiment is exemplified by the case where the darkest signal in the image area ARN is lowered to a pedestal level, however, the present invention 40 is not necessarily limited thereto, and hence it may be lowered to a predetermined level.

Next, another preferred embodiment will be described.

An example where the present invention is applied not to a high vision television system but to a conventional television system will be described. When a cinema size picture which is enhanced in its reality and impression because of its width, is displayed on a conventional television system, it will be a familiar picture as illustrated in FIG. 5.

The dynamic picture function can also be applied to this picture by forming a black level detection signal S3 (FiG. 5B) and a blanking pulse signal S4 (FIG. 5C).

The operation will be described in detail.

When the block level detection signal S3 inputted from $_{55}$ the black detection pulse input terminal 4 falls, the black level hold circuit 3 detects and holds the darkest signal level in input video signal V_{IN} . When the black level detection signal S3 rises, the black level hold circuit 3 stops detecting the darkest signal level in the input video signal V_{IN} .

The black level detection signal S3 lowers in the area ARN where the signal is displayed in cinema size (hereinafter referred to as cinema size area) which is within the area ARAX where the NTSC video signal is displayed (hereinafter referred to as NTSC picture display area), whereas it 65 rises at the black margin area ARB at the border of the screen (FIG. 5B).

The black level hold circuit 3 holds the darkest signal level within the cinema size area ARNX, thereby preventing the near black signal in the top and bottom black margin area ARBX instead of the darkest signal in the cinema size area ARNX from being detected.

The black level correction circuit 1, by varying the resistance of resistor R3 and the capacitance of capacitor C1, changes the time constant and sets the pulse width of the darkest signal that the black level hold circuit 3 can detect from the input video signal V_{IN} .

The black level expansion circuit 6, while the blanking pulse S4 inputted from the blanking pulse input terminal 7 lowers, i.e. while it is outside the blanking period, lowers the detected black signal level to the pedestal level.

Here, the blanking pulse signal S4 lowers through out the entire screen display period.

Therefore, when the average brightness level in the cinema size area ARNX is high such that the display is bright, the circuit lowers the darkest detected video signal V_{IN} to the pedestal level, thereby preventing the black signal portion from seemingly floating even when the black signal portion is small.

Also because of this, the brightness level of the input video signal throughout the display screen can be lowered, thereby preventing the border between the cinema size area ARNX and the black margin area ARBX from being noticeable when the darkest signal level in the cinema size area ARNX and the black margin area ARBX are equal.

When the average brightness level of the input video signal V_{IN} is high and does not have much black signal, the black level hold circuit, because the area of the black signal (shown with oblique lines in the cinema size area ARNX in FIG. 6A) within the cinema size area ARNX is small compared to the area of the inputted video signal V_{IN} , does not hold the black signal portion as the darkest black signal level, and instead, holds the white level signal as the black level. Here, the black level expansion circuit 6, because the blanking pulse signal S4 is dropping, expands only the black signal portion of the video signal V_{IN} within the cinema size area and thereby corrects the video signal so as to make it look more black.

As described above, according to the present invention, when an image is displayed in a first display screen having a first aspect ratio, the black level of a video signal is lowered to a predetermined level covering an overall display screen, thereby avoiding effectively a probability that a boundary of a second display screen and an extra area outward of the second display screen is sensed visually.

Further, when an image are displayed in the second display screen having a second aspect ratio, a black signal in a video signal is detected only within the second display screen, and the black signal is not detected in the extra screen, therefore a black level in the second display screen can be lowered to a predetermined level.

While there has been described in connection with the preferred embodiments of the invention, it will be obvious to those skilled in the art that various changes and modifications may be made therein without departing from the invention, and it is aimed, therefore, to cover in the appended claims all such changes and modifications as fall within the true spirit and scope of the invention.

What is claimed is:

- 1. A display unit, comprising:
- a first display screen area having a first aspect ratio; a second display screen area having a second aspect ratio;

- a black frame area partially bordering said second display screen area;
- signal level expansion means for lowering a darkest signal level in an image of a display unit to a predetermined level when said image is displayed in said first display 5 screen area;
- signal level detecting means for detecting a darkest signal level of an image in said second display screen area when said image is displayed in said second display screen area, said signal level detecting means ignoring said black frame area when detecting a darkest signal level; and
- said signal level expansion means lowering a darkest signal level in an image of said display unit to a predetermined level when said image is displayed on said second display screen area based on a detected result of said signal level detecting means.
- 2. A display unit as claimed in claim 1, wherein said first aspect ratio is further defined by a 16 to 9 aspect ratio, and wherein said second aspect ratio is further defined by a 4 to 3 aspect ratio.
 - 3. A display unit comprising:
 - a first display screen having a first aspect ratio;
 - a second display screen having a second aspect ratio;
 - a black frame area partially bordering said second display screen;
 - signal level detection means for detecting a darkest signal level of an image in said second display screen when said image is displayed in said second display screen; and
 - signal level expansion means, electrically connected to said signal level detection means, for lowering said

- darkest signal level to a predetermined level based on a detected result of said signal level detection means.
- 4. A display unit as claimed in claim 3, wherein said first aspect ratio is further defined by a 16 to 9 aspect ratio, and wherein said second aspect ratio is further defined by a 4 to 3 aspect ratio.
- 5. A display unit as claimed in claim 3, further comprising variable time constant means for varying the pulse width of said darkest signal level detected by said signal level detection means, said variable pulse width means being electrically connected to said signal level detection means and to said signal level expansion means.
- 6. A method for lowering a black level in a display unit comprising the steps of:
 - setting a first black level in a first display screen having a first aspect ratio;
 - setting a second black level and a second display screen having a second aspect ratio;
 - detecting a darkest signal of a video signal from an image area corresponding to said second display screen, excepting a black frame region partially bordering said second display screen; and
- lowering said darkest signal to a predetermined level in an image area corresponding to said first display screen.
- 7. A method as claimed in claim 6, wherein said first aspect ratio is further defined by a 16 to 9 aspect ratio and wherein said second aspect ratio is further defined by a 4 to 3 aspect ratio.
- 8. A method as claimed in claim 6, further comprising the step of varying a pulse width of said darkest signal level.

UNITED STATES DISTRICT COURT CENTRAL DISTRICT OF CALIFORNIA

NOTICE OF ASSIGNMENT TO UNITED STATES MAGISTRATE JUDGE FOR DISCOVERY

This case has been assigned to District Judge Alicemarie H. Stotler and the assigned discovery Magistrate Judge is Arthur Nakazato.

The case number on all documents filed with the Court should read as follows:

SACV08- 1135 AHS (ANx)

Pursuant to General Order 05-07 of the United States District Court for the Central District of California, the Magistrate Judge has been designated to hear discovery related motions.

All discovery related motions should be noticed on the calendar of the Magistrate Judge
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NOTICE TO COUNSEL
opy of this notice must be served with the summons and complaint on all defendants (if a removal action is

A copy of this notice must be served with the summons and complaint on all defendants (if a removal action is filed, a copy of this notice must be served on all plaintiffs).

Subsequent documents must be filed at the following location:

Western Division			
 312 N. Spring St., Rm. G-8			
Los Angeles, CA 90012			

[X] Southern Division 411 West Fourth St., Rm. 1-053 Santa Ana, CA 92701-4516

Eastern Division 3470 Twelfth St., Rm. 134 Riverside, CA 92501

Failure to file at the proper location will result in your documents being returned to you.

Steven M. Anderson (Bar No. 144014) QUINN EMANUEL URQUHART OLIVER & HEDGES, LLP 865 S. Figueroa Street, 10th Floor Los Angeles, California 90017 tel: (213) 443-3000

•	DISTRICT COURT CT OF CALIFORNIA
SONY CORPORATION, A Japanese corporation,	CASE NUMBER
PLAINTIFF(S) v. VIZIO, Inc.,	SACV08-1135 AHS (A
DEFENDANT(S).	SUMMONS
TO: DEFENDANT(S): VIZIO, Inc. A lawsuit has been filed against you. Within 20 days after service of this summon must serve on the plaintiff an answer to the attached of counterclaim cross-claim or a motion under Rule 12 or motion must be served on the plaintiff's attorney, Stempton Street, 10th Floor, Los Angeles, Califor judgment by default will be entered against you for the regour answer or motion with the court.	2 of the Federal Rules of Civil Procedure. The answer even M. Anderson , whose address is mia 90017 . If you fail to do so,
OCT 1 0 2008	Clerk, U.S. District Court By:
[Use 60 days if the defendant is the United States or a United States 50 days by Rule 12(a)(3)].	agency, or is an officer of smoothy of the United States. Allowed

CV-01A (12/07)

UNITED STATES DISTRICT COURT, CENTRAL DISTRICT OF CALIFORNIA CIVIL COVER SHEET

FOR OFFICE USE ONLY: Case Number:

AFTER COMPLETING THE FRONT SIDE OF FORM CV-71, COMPLETE THE INFORMATION REQUESTED BELOW.

CV-71 (05/08)

UNITED STATES DISTRICT COURT, CENTRAL DISTRICT OF CALIFORNIA CIVIL COVER SHEET

VIII(a). IDENTICAL CASES: Has If yes, list case number(s):	s this action been pr	eviously filed in this court and	l dismissed, remanded	or closed? 🕏 No	□ Yes	
VIII(b). RELATED CASES: Have If yes, list case number(s): CV08-0	e any cases been pre 3934 RGK (FMO	viously filed in this court that	are related to the pres	ent case? 🗆 No	of Yes	
₫ C.	Arise from the same Call for determinati For other reasons w		related or similar que tion of labor if heard b	stions of law and t by different judges	; or	
IX. VENUE: (When completing the					, , , , , , , , , , , , , , , , , , , ,	
(a) List the County in this District; ☐ Check here if the government, it	California County o is agencies or emplo	utside of this District, State if one of the state if the open is a named plaintiff. If the open is a named plaintiff.	other than California; his box is checked, go	or Foreign Countr to item (b).	y, in which EACH named plaintiff resides.	
County in this District:*			California County outside of this District; State, if other than California; or Foreign Country			
			Sony Corporation: o	citizen of Japan;		
(b) List the County in this District; Check here if the government, it	California County o s agencies or emplo	utside of this District; State if o yees is a named defendant. If	other than California; this box is checked, g	or Foreign Countr o to item (c).	y, in which EACH named defendant resides.	
County in this District:*			California County outs	ide of this District;	State, if other than California; or Foreign Country	
VIZIO, Inc Orange County, Co						
(c) List the County in this District; (Note: In land condemnation ca	California County or uses, use the locatio	utside of this District; State if one of the tract of land involved	other than California;	or Foreign Country	y, in which EACH claim arose.	
County in this District:*			California County outs	ide of this District;	State, if other than California; or Foreign Country	
Claims 1-14: Los Angeles Count	у					
* Los Angeles, Orange, San Bernar Note: In land condemnation cases, us	dino, Riverside, Ve e the location of the	entura, Santa Barbara, or Santast of land involved	n Luis Obispo Count	ies		
X. SIGNATURE OF ATTORNEY (OR PRO PER);	Steven M	len)	Date Octobe	r 10, 2008	
or other papers as required by law but is used by the Clerk of the Co	v. This form, approve ourt for the purpose o	ed by the Judicial Conference of	of the United States in .	September 1974, is	or supplement the filing and service of pleadings sequired pursuant to Local Rule 3-1 is not filed ed instructions, see separate instructions sheet.)	
Key to Statistical codes relating to So-	cial Security Cases:					
Nature of Suit Code	Abbreviation	Substantive Statement of C	Cause of Action			
861	НІА	All claims for health insurance benefits (Medicare) under Title 18, Part A, of the Social Security Act, as amended. Also, include claims by hospitals, skilled nursing facilities, etc., for certification as providers of services under the program. (42 U.S.C. 1935FF(b))				
862	BL	All claims for "Black Lung" benefits under Title 4, Part B, of the Federal Coal Mine Health and Safety Act of 1969. (30 U.S.C. 923)				
863	DIWC	All claims filed by insured workers for disability insurance benefits under Title 2 of the Social Security Act, as amended; plus all claims filed for child's insurance benefits based on disability. (42 U.S.C. 405(g))				
863	DIWW	All claims filed for widows or widowers insurance benefits based on disability under Title 2 of the Social Security Act, as amended. (42 U.S.C. 405(g))				
864 ·	SSID All claims for supplemental security income payments based upon disability filed under Title 16 of the Social S Act, as amended.					
RSI All claims for retirement (old age) and survivors benefits under Title 2 of the Social Security Act, as amended U.S.C. (g))					2 of the Social Security Act, as amended. (42	

CIVIL COVER SHEET

Page 2 of 2

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